ELECTRICAL CHARACTERIZATION OF TRANSPARENT CONDUCTOR - OXIDE - SEMICONDUCTOR (TCOS) SURFACE BARRIER DEVICES

A Thesis Submitted
In Partial Fulfilment of the Requirements
for the Degree of

DOCTOR OF PHILOSOPHY

by
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to the

INTERDISCIPLINARY PROGRAMME IN MATERIALS SCIENCE
INDIAN INSTITUTE OF TECHNOLOGY, KANPUR
AUGUST 1984

CERTIFICATE

This is to certify that the thesis entitled 'Electrical Characterization of Transparent Conductor-Oxide-Semiconductor (TCOS) Surface Barrier Devices' by Sudhanshu Varma is a record of work carried out under my supervision and has not been submitted elsewhere for a degree.

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ACKNOWLEDGEMENTS

I would like to take this opportunity to express my sincere gratitude to Professor S. Kar for his excellent guidance and constant encouragement throughout the course of this work. My association with him during the past ten years has been very rewarding and I feel privileged to have worked with him.

I wish to thank Dr. S. Ashok of Pennsylvania State University, University Park, U.S.A. for providing the spray deposited samples for interface investigations. My thanks are also due to Mr. P. Saraswat for his help during measurement and analysis of spray deposited samples.

I am very much thankful to Dr. K.V. Rao for his help during deposition and characterization of transparent conductor films.

I would also like to thank Mr. R.L. Narasimhan for his help in analysis of admittance data for conductance technique. Assistance rendered by Ms Manju Tewari, Ms Asha Pandey and Ms Sushama Saxena at various stages is also acknowledged.

I wish to thank all my friends for their direct and indirect help during the course of this work. I am also thankful to Mr. C.M. Abraham for excellent typing of the manuscript.

Financial assistance from National Science Foundation, U.S.A., vide Grant INT-8012203, during the course of this work is gratefully acknowledged.

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SYNOPSIS

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'ELECTRICAL CHARACTERIZATION OF TRANSPARENT CONDUCTOR-OXIDE-SEMICONDUCTOR (TCOS) SURFACE BARRIER DEVICES'

The primary objective of the present investigation was to study surface defects in transparent conductor-oxide-semiconductor (TCOS) devices prepared by physical (e-beam deposition), as well as chemical (CVD and spray) deposition processes, and to investigate the effect of illumination on these defects.

Chemical vapor deposition was carried out in a standard tube furnace to deposit undoped and Sb- doped SnO_2 films using hydrolysis of chlorides. Deposition temperature was 300°C and deposition rates were 10-30 Å/min. Undoped SnO_2 films had resistivity of the order of 3×10^{-3} Ohm-cm, while Sb-doped films had resistivity of the order of $1.0-2.0 \times 10^{-3}$ Ohm-cm. Lowest value of resistivity was 8.6×10^{-4} Ohm-cm for a 1430 Å thick Sb-doped SnO_2 film . Optical transmission was 90-95% for incident radiation wavelength of 0.4-1.8 μm. Optical bandgap of Sb-doped SnO_2 film was 3.97 eV. X-ray investigations showed preferred orientation and presence of SnO_2 and SnO (O) phases in undoped films and additional Sb_2O_5 and

Sb_2O_4 phases in Sb-doped films. Grain size was 900-1450 Å for undoped films and 540-720 Å for Sb-doped films.

Electron-beam deposition of Sn-doped In_2O_3 at 300°C in residual air atmosphere resulted in opaque film requiring post-deposition oxidation step, after which the sheet resistance was about 30-60 Ohm/sq. Deposition in oxygen partial pressure of $5x10^{-6}$ Torr eliminated the need for post-deposition oxidation and resulted in sheet resistance of 20-25 Ohm/sq. Increase in oxygen partial pressure increased sheet resistance. Films deposited under oxygen partial pressure were very stable and subsequent annealing at 400-550°C in oxidizing or reducing ambient for 60 min or more did not alter film resistivity appreciably.

Identification of the dominant current transport mechanism in chemical vapor deposited SnO_2-nSi heterojunctions was carried out by measuring I-V and C-V characteristics at various temperatures. Undoped sample had recombination-generation as the dominant carrier process while Sb-doped sample had multi-step tunneling as the main current transport mechanism. Undoped sample indicated lower trap density compared to Sb-doped sample whose reverse bias C^{-2}-V characteristics showed varying slopes with bias and temperature indicating different levels of traps.

Suitability of transparent conductor-oxide-semiconductor (TCOS) structure for interface investigation has been demonstrated. A technique for obtaining reliable information about

interface states by MOS admittance measurements under illumination has been developed. It has been shown that simultaneous use of capacitance and conductance data under illumination can make data analysis simple and reliable. Three simple and direct methods have been presented which can directly give quasi-Fermi level separation from measured high frequency or low frequency C-V characteristics - in dark and under illumination. The knowledge about state capture cross-sections for majority and minority carriers from admittance data under illumination was found essential to accurately determine the dominant imref at a particular interface potential.

Interface investigations in TCOS structures under illumination, prepared by spray deposition, chemical vapor deposition, and e-beam deposition, have been carried out by the procedure developed. The conductance technique could not be used for interface investigation in spray and chemical vapor deposited samples due to high series resistance. In the absence of experimental data about σ_h and σ_e, the issue of hole vs electron exchange was resolved in the following manner. Since the uncertainity due to lack of knowledge of σ_h and σ_e in interface potential is about 0.12 V on each side of the interface potential, at which the quasi-Fermi levels are equidistant from the midgap, the states near a band edge were assumed to exchange charge with the corresponding band. Also, all the states giving rise to a peaked state density distribution were assumed to exchange charge with the band whose edge

was nearer to the location of interface state density peak, provided the location of the peak was outside the interface potential region where dominant imref was uncertain. Conductance technique could be used in case of e-beam deposited samples and dominant imref was determined by finding whether the product $n_s\sigma_e$ was greater than $p_s\sigma_h$ or not. In the former case the electron imref will dominate, otherwise the hole imref will dominate. Interface state density profile obtained by capacitance technique matched well with the values obtained by conductance technique indicating that the assumptions made in capacitance data analysis are correct. The results indicate presence of interface state density peak, located around 0.30-0.45 eV above valence band, overlying the usual U shaped background state density profile in case of all the samples. E-beam sample on p-Si showed an additional N_{is} peak located around 0.30 eV below conduction band. The magnitude of these peaks increased and their location shifted towards band edge with increasing illumination level. This indicated generation of additional traps due to optically assisted process. No permanent photon damage was observed under illumination and the observed behaviour was totally reversible. Conductance data indicated that $\sigma_h >> \sigma_e$ for e-beam deposited sample on p-Si. The capture cross-sections were also found to vary with band-energy.

CHAPTER 1

INTRODUCTION

Transparent conductors, as the name suggests, possess high transparency and good electrical conductivity simultaneously. Ultrathin metal films have been used since long in various applications like photoelectric cells [1] and Schottky barrier photodetectors [2] due to their semitransparent nature. They have also been used in various metal-oxide-semiconductor (MOS) solar cells fabricated during 1970s [3]. Difficulty in reproducing the properties of these ultrathin metal films, and their poor mechanical and chemical stabilities, have diverted the attention of investigators to oxide semiconductors, which are generally referred to as transparent conductors. The simultaneous occurrence of transparency and electrical conductivity in thin film of an oxide semiconductor, CdO, was first reported in 1907 [4]. The commercial use of such films was generated by aircraft industries in 1940s which needed transparent electrical heaters for windshield deicing. Since then, considerable amount of research has been done on transparent conductors. The increasing interest in the interaction of light with electronic materials and devices has made transparent conductors a very important category of electronic materials.

Lack of understanding of transparent conducting behaviour led to many contradictory results during early investigations which have been reviewed by Holland [5]. Systematic investigations later on led to useful results on the properties of transparent conducting films (generally 0.1 to 1.0 μm thick) which have been reviewed by Vossen [6], Haacke [7], Manifacier [8], and Chopra et al [9]. The oxide semiconductors mostly studied include CdO, SnO_2, In_2O_3, Cd_2SnO_4, $CdSnO_3$ and ZnO; and their properties investigated include transparency, electrical conductivity, bandgap, refractive index, structure and morphology, chemical nature, environmental stability, etc [6-9], which are summarised below. These materials generally have band gaps in the range of 3.0 - 4.0 eV resulting in high transparency (80% - 95%) in visible spectrum of light. The n-type conductivity arises due to nonstoichiometry in the films resulting in presence of oxygen ion vacancies and/or interstitial impurity ions. The conductivities have been found to improve by using suitable dopants like Sb and F for SnO_2 films and Sn for In_2O_3 films. The conductivities obtained are generally in the range of 10^2 to 10^4 mho cm^{-1} with carrier concentrations more than 10^{20} cm^{-3}. Such high carrier concentrations make these semiconductors degenerate and result in good infrared reflecting properties. The refractive indices are reported to be around 2.0 which make these films very good antireflection coatings on silicon solar cells.

Apart from transparent heaters for aircraft/automobile wind-shields, the transparent conductors have found variety of applications [6-9]. These are : infra-red reflector for glass windows and incandescent bulbs, antistatic coatings for instrument panels, gas sensors, protective and wear-resistant coatings for glass containers, low temperature secondary thermometers, thin film resistors, antireflection coatings, reflector absorber tandem for photothermal conversion, transparent electrodes for display devices like liquid crystal displays and light emitting diodes, imaging tubes (vidicons), transparent gates for various opto-electronic devices like photodetectors, solar cells and solid state imaging devices, etc. Each application requires a different emphasis on various properties of transparent conductors. Knowledge about transparency, conductivity, mechanical hardness and chemical (environmental) stability may be sufficient for passive applications. Active applications, on the otherhand, require more detailed knowledge about electrical, optical, structural and chemical properties. Our interest lies in application of transparent conductors in electronic devices. These devices, till date, have mostly employed SnO_2 or In_2O_3 films.

Transparent conductors have been deposited by various chemical and physical processes [6,8,9]. These include: chemical vapor deposition, spray hydrolysis, chemical solution growth, dip technique, oxidation of metallic films, reactive

evaporation, direct evaporation of oxides, reactive ion plating, reactive sputtering, magnetron sputtering, d.c./r.f. sputtering from oxide targets, ion beam sputtering, etc. Spray hydrolysis has been the most extensively used process for depositing SnO_2 films for many applications. Because of ease in coating large areas, adaptability to automation, and low cost materials used, it has been found very promising for solar cell applications. Solar cells with efficiencies exceeding 14% have been reported to be fabricated with spray deposition of SnO_2 and In_2O_3 films on n-type Si [10]. Ion-beam sputtered In_2O_3-SiO_x-pSi solar cells have yielded efficiencies in the range of 13-16% [11,12]. Polycrystalline silicon solar cells using transparent gates have resulted in efficiencies in the range of 10-12% [13]. Electron-beam evaporated In_2O_3-pCdTe heterojunction solar cells have been reported with 10.5% efficiency [14]. Electron-beam deposited In_2O_3-p$CuInSe_2$ [15], and r.f. sputtered In_2O_3-pCdTe [16] and ZnO-pCdTe [16] solar cells yielded efficiencies in the range of 8-9%. In_2O_3-pInP solar cell prepared by ion beam deposition has also been reported with an active area efficiency of 14.4% [17]. In addition to solar cells, the transparent conductors have also been used in fabrication of high efficiency photodetectors [18], charge couple devices [19,20], and charge injection devices [21,22], which are used as solid state imaging devices. SnO_2 films used in the case of charge injection

devices were deposited by sputtering [21] and chemical vapor deposition [22], while In_2O_3 films used in photodetectors [18], charge coupled devices [19,20], and charge injection devices [21] were sputter deposited.

Most of the investigations reported till now were aimed at deposition of transparent conducting films by various techniques and study of their electrical, optical, structural, and chemical properties [6-9]. Transparent conductor-silicon (and a few other semiconductors) heterojunction solar cells prepared by various techniques have also been studied extensively so as to achieve as high efficiency as possible [10-17]. Application of transparent conductors in other electronic devices like solid state imaging devices, etc. is also being investigated [18-22]. The performance of all these surface barrier devices is governed by the presence of traps and interface states. The role of these traps and interface states under illumination becomes very important for electronic devices involving interaction with light. Very little, however, has been reported on the generation of these defects by various deposition techniques, and the materials used for chemical deposition processes, and the effect of illumination on these defects. The primary objective of this investigation was the study of interface states, under illumination, in transparent conductor-oxide-silicon surface barrier devices prepared by various deposition techniques like spray hydrolysis, chemical

vapor deposition,and electron beam evaporation. The generation of traps in transparent conductor-silicon heterojunctions prepared by chemical vapor deposition, their dependence on the materials used during deposition, and their role in governing carrier transport processes across the heterojunction has also been investigated.

Spray hydrolysis of chlorides to form SnO_2 and In_2O_3 films, has been extensively used in fabrication of solar cells [10]. However, for more sophisticated applications like solid state imaging devices, spray hydrolysis may not be suitable, as the problems with uniformity and reproducibility are frequently encountered. Chemical vapor deposition is expected to give more uniform and reproducible films, making it attractive for electronic device applications. Chemical vapor deposition can be done either by pyrolysis of organometallic compounds or by hydrolysis of chlorides. We have chosen to study the films deposited by chemical vapor deposition using hydrolytic reaction as the reagents used are same as those used in spray deposition. The films have been deposited on silicon and silica substrates in a standard tube furnace. The electrical resistivity, optical transparency, and structural properties like grain size and various phases present in the film, have been studied for undoped and Sb doped SnO_2 films. The aim was to deposit films with low electrical resistivity and high optical transparency so that they could be used to make SnO_2-silicon

heterojunctions and SnO_2-SiO_2-Si (TCOS) structures for studies on traps and interface states. The structural characterization was done to get an idea about various phases present in the film which could help in determining the origin of traps. No systematic attempt was made to study the variation in film properties with deposition parameters, as that was not within the scope of this work. Electron beam evaporation from oxide target has been used to deposit Sn doped In_2O_3 films on silicon and silica substrates. These films have been deposited in residual gas atmosphere as well as in oxygen partial pressure. The effect of post-deposition heat treatments in residual gas atmosphere, inert ambient, oxidizing ambient, and reducing ambient, have been studied. The details of film deposition by chemical vapor deposition and electron beam deposition, and their characterization are given in Chapter 2.

An interesting feature that we have observed in case of SnO_2 (or In_2O_3)-nSi solar cells, prepared by spray hydrolysis, is their consistently high open-circuit voltage, but the fill factors have been comparatively low. Low fill factors arise due to excess diode current in solar cells. The chemical processes, like hydrolysis, are likely to introduce traps at the interface and in depletion region. These traps may be generated due to various chemical species present during the reaction, which might either be from the reagents used or as a result of by-products of reactions. Similarly, physical

processes like sputtering and evaporation may give rise to radiation damage at the interface, arising from striking of the interface by the charged particles and X-rays etc, during deposition. These traps and interface states can play a dominant role in governing the carrier transport process across the barrier. It is, therefore, important to investigate the current transport mechanism in transparent conductor-silicon heterojunctions. Though some attempts have been made to identify the dominant carrier transport process in these heterojunctions [14,23-28], they have led to doubtful conclusions in a few cases due to incomplete investigations [23-25]. We have prepared SnO_2-Si and Sb doped SnO_2-Si heterojunctions by chemical vapor deposition, and have demonstrated how the dominant current transport mechanism can be identified, based on the presently available diagnostic tools, from the current vs voltage and capacitance vs voltage characteristics measured at different temperatures. The reason for investigating the carrier transport mechanism in case of chemical vapor deposited heterojunctions is that, this study can also be helpful in identifying the source of undesired diode current in spray deposited solar cells, since the reagents and reactions remain same for both these deposition techniques. Moreover such studies, on chemical vapor deposited SnO_2-Si heterojunctions, have not been reported in literature. The effect of traps, generated by the chemical processing, on the heterojunction

barrier and transport process, and the possible origin of these traps have also been investigated [29]. Such an information can help in minimizing the factors responsible for excess diode current, and the fill factors can be improved further, resulting in higher efficiencies in these solar cells. Chapter 3 gives details of these investigations.

The physical processes like sputtering and electron beam deposition, which are commonly used in fabrication of modern microelectronic devices, are known to cause surface defects by irradiation with energetic particles like ions, electrons, photons (X-rays), etc. This results in additional interface states at thermally grown SiO_2--Si interface, and in degradation of SiO_2, which govern the behaviour of these devices. Though some studies have been carried out to determine the density of these defects, and their thermal annealing in various ambients [18,30-39], very little has been reported on the nature and origin of these defects. The effect of illumination on the behaviour of these defects becomes important for optoelectronic devices like solar cells and solid state imagers and needs to be studied. Similarly, no interface investigation has been reported on chemically deposited (spray or chemical vapor deposition) transparent conductor-oxide-silicon (TCOS) structures, which is also important for opto-electronic devices. We, therefore, decided to characterize

$Si-SiO_2$ interface in TCOS structures under illumination, which were prepared by physical (e-beam evaporation) as well as chemical (spray and CVD) processes.

The most important aspect of present interface investigation was to develop a procedure for obtaining reliable information about interface states by small signal admittance measurements under illumination. The use of illumination to determine interface state distribution in the minority carried bandgap half, and to determine interface state capture cross-sections for minority carriers, by conductance technique, was demonstrated by Poon et al. [40,41]. The knowledge about quasi-Fermi level separation becomes important for obtaining interface state profile from admittance measurements under illumination, and the technique proposed by Poon et al [41] involves calculation of the semiconductor space charge as a function of the surface potential for a range of values of quasi-Fermi level separation. We have demonstrated the suitability of TCOS structures for $Si-SiO_2$ interface investigation, under illumination, by the capacitance technique which is simpler compared to conductance technique [42]. We have also presented three simple and direct methods for experimentally determining quasi-Fermi level separation from measurement of either high or low frequency capacitance-voltage characteristics of a TCOS structure in dark and under illumination [43,44]. In case of interface investigation in dark,

either the capacitance or the conductance, technique can be used to get reliable data on interface states. However, we have shown that in order to get reliable information about interface states and their capture, cross sections under illumination, the conductance technique should be used alongwith the capacitance technique. The details of the technique proposed are given in Chapter 4.

Use of illumination extends the capabilities of admittance techniques for obtaining additional information about interface states. In dark the interface states generally exchange charge with the majority carrier band. Information about interface states near the minority carrier band edge cannot be obtained by quasi-static technique, specially if they have small capture cross-section for majority carriers, because of problems with leakage current, device drift, and long time periods necessary. These states can be accessed easily under illumination. Thus interface states over most of the bandgap can be characterised by admittance techniques with help of illumination. Measurements under illumination yield electron capture cross-section (σ_e) of upper half bandgap states and hole capture cross-section (σ_h) of lower half bandgap states. These capture cross-sections may not be equal and knowledge of both may help in identifying the nature of traps, e.g., acceptor traps will result in $\sigma_h >> \sigma_e$.

Use of illumination also helps in finding optically activated states, their nature, and behaviour under different illumination levels [44]. Knowledge about interface state distribution under illumination becomes important in the above context. Interface investigation in case of ultrathin oxides for VLSI applications can be carried out by quasi-static technique only at high ramp rate due to large leakage currents. This does not give information about a large number of states which cannot respond to high ramp rates. In such cases capacitance-voltage and conductance-voltage measurements under illumination can be used to get interface state profile. Interface investigations were carried out using admittance techniques under illumination, on TCOS structures prepared by spray hydrolysis, chemical vapor deposition, and electron beam evaporation. Effect of illumination on these interface states was also studied by varying the illumination level. Such a study is expected to yield very useful results for solid state imaging devices. Details of the procedures outlined for interface investigations, using TCOS structures under illumination, and the results obtained are given in Chapter 4.

In addition to providing capture cross-sections for upper half and lower half band gap states, the conductance technique can also give the break up if states with different capture cross-sections are present in the same region. Capacitance technique data provides the sum total of the densities of such a collection of states but the conductance technique can break this up into groups having different capture cross-sections and provide the density of each group. In fact the biggest handicap of conductance technique previously was the large time taken for measurement and data analysis, which now has been overcome by powerful equipment like HP 4192A LF impedance analyser with facilities for automation and interfacing with desk top computer. Conductance voltage measurements at a large number of frequencies over a wide frequency range under different illumination levels and the data analysis can now be done in a short time to get useful information about interface defects.

References

1. C. Bidwell, Philos. Mag. 20, 178 (1885).

2. L. Bergmann, Phys. Z. 32, 286 (1931).

3. S. Kar, D. Shanker, S.P. Joshi and S. Bhattacharya, Proc. 13th IEEE Photovoltaic Specialists Conf. 628(1978).

4. K. Badeker, Ann. Phy. (Leipzig) 22, 749 (1907).

5. L. Holland, 'Vacuum Deposition of Thin Films', (Wiley, New York, 1958).

6. J.L. Vossen, Phys. Thin Films 9, 1 (1977).

7. G. Haacke, Annu. Rev. Mater. Sci. 7, 73 (1977).

8. J.C. Manifacier, Thin Solid Films 90, 297 (1982).

9. K.L. Chopra, S. Major and D.K. Pandya, Thin Solid Films 102, 1 (1983).

10. T. Feng, D.J. Eustace and A.K. Ghosh, Proc. 16th IEEE Photovoltaic Specialists Conf., XX (1982).

11. J. Schewchun, J. Dubow, C.W. Wilmsen, R. Singh, D. Burk and J.F. Wager, J. Appl. Phys. 50, 2832 (1979).

12. P.P. Sharma, T.C. Anthony, S. Ashok, S.J. Fonash and L.L. Tongson, Jpn. J. Appl. Phys. 19 (Suppl.1), 551 (1980).

13. R. Singh, M.A. Green, and K. Rajkanan, Solar Cells 3, 95 (1981).

14. J.G. Werthen, A.L. Fahrenbruch, R.H. Bube and J.C. Zesch, J. Appl. Phys. 54, 2750 (1983).

15. L.L. Kazmerski and P. Sheldon, Proc. 13th IEEE Photovoltai Specialists Conf., 541 (1978).

16. A.L. Fahrenbruch, J. Aranovich, F. Courreges, T. Chynoweth, and R.H. Bube, Proc. 13th IEEE Photovoltaic Specialists Conf., 281 (1978).

17. K.J. Bachman, H. Schreiber (Jr), W.R. Sinclair, P.H. Schmidt, F.A. Thiel, E.G. Spencer, G. Pasteur, W.L. Feldman, and K. Sree Harsha, J. Appl. Phys. 50, 3441 (1979).

18. D.K. Schroder, IEEE Trans. Electron Devices ED-25, 90 (1978).

19. L.L. Thompson, D.H. McCann, R.A. Tracy, F.J. Kub and M.H. White, IEEE Trans. Electron Devices ED-25, 132(1978).

20. D.H. McCann, A.P. Tulrley, J.A. Hall, J.M. Walker, R.A. Tracy and M.H. White, Proc. Int. Solid State Circuits Conf., 30 (1978).

21. D. Brown, M. Ghezzo and M. Garfinkel, IEEE J. Solid State Circuits SC-11, 128 (1976).

22. D. Brown, M. Ghezzo and P.M. Sargent, IEEE Trans. Electron Devices, [illegible] (1978).

23. H. Kato, J. Fujimoto, T. Kanda, A. Yoshida, and T. Arizumi, Phys. Stat. Sol. 32, 255 (1975).

24. T. Feng, C. Fishman and A.K. Ghosh, Proc. 13th IEEE Photovoltaic Specialists Conf., 519 (1978).

25. A.K. Ghosh, C. Fishman and T. Feng, J. Appl. Phys. 49, 3490 (1978).

26. T. Nagatomo, M. Endo, and O. Omoto, Jpn. J. Appl. Phys. 18, 1103 (1979).

27. S. Ashok, P.P. Sharma, and S.J. Fonash, IEEE Trans. Electron Devices ED-27, 725 (1980).

28. N.S. Chang and J.R. Sites, J.Appl.Phys. 49,4833 (1978).

29. S. Varma, K.V. Rao, and S. Kar, J. Appl. Phys. 55, July (1984).

30. D.R. Collins and C.T. Sah, Appl. Phys. Letters 8, 124 (1966).

31. D.V. Mccaughan and R.A. Kushner, Proc. IEEE 62, 1236 (1974).

32. A.K. Sinha, J. Electrochem. Soc. 123, 66 (1976).

33. T.H. Ning, J.Appl.Phys. 49, 4077 (1978).

34. H.S. Lee, IEEE Trans. Electron Devices ED-25, 795(1978).

35. M. Pockerar, R. Fulton, P. Blaise, D. Brown, and R. Whitlock, J. Vac. Sci. Technol. 16, 1653 (1979).

36. R.A. Gdula, IEEE Trans. Electron Devices ED-26, 644 (1979).

37. S. Alexandrova, K. Kirov and A. Szekeres, Thin Solid Films 75, 37 (1981).

38. T. Ando, and C.K. Fong, IEEE Trans. Electron Devices ED-29, 1161 (1982).

39. S.W. Pang, D.D. Rathman, D.J. Silversmith, R.W. Mountain, and P.D. DeGraff, J. Appl. Phys. 54, 3272 (1983).

40. T.C. Poon and H.C. Card, J. Appl. Phys. 51, 5880 (1980).

41. T.C. Poon and H.C. Card, J. Appl. Phys. 51, 6273 (1980).

42. S. Kar, S. Varma, P. Saraswat and S. Ashok, J. Appl.Phys. 53, 7039 (1982).

43. S. Kar and S. Varma, J. Appl. Phys. 54, 1988 (1983).

44. S. Kar and S. Varma, To be published.

CHAPTER 2

DEPOSITION AND CHARACTERIZATION OF TRANSPARENT CONDUCTING FILMS

2.1 INTRODUCTION

Various thin film deposition techniques have been used for deposition of transparent conducting films. These include physical deposition processes like sputtering and evaporation, and chemical deposition processes like spray hydrolysis and chemical vapor deposition. Different deposition techniques, and the deposition parameters governing the film properties, have been reviewed by Vossen [1] and Chopra et al [2].

The properties of transparent conducting films, deposited by various techniques, show a marked scattering in the literature, since the thin film properties are governed by various deposition parameters. The most important properties are sheet resistance and transmittance. They are given by [2] :

$$R_{sh} = \frac{\rho(t)}{t} = \frac{1}{\sigma(t)\, t} \qquad (2.1)$$

and

$$T_\lambda = (1-R_\lambda)^2 \exp(-\alpha_\lambda\, t) \qquad (2.2)$$

where R_{sh} is the sheet resistance of the film, t is the film thickness, $\rho(t)$ [or $\sigma(t)$] is the resistivity [or conductivity],

If this quantity is called C'_{FB} it can be expressed by

$$C'_{FB} = \frac{1}{x_{ox}/\varepsilon_{ox} + [kT/q^2 \varepsilon_s N_a]} = \frac{1}{1/C'_{ox} + L_D/\varepsilon_s} \qquad (2.10)$$

where L_D is the extrinsic Debye length.

When the gate voltage becomes more positive than the flat-band voltage, holes are repelled from the surface of the silicon and the system is in the depletion-bias condition. Under this condition, relatively straightforward electrostatic analysis shows that the overall capacitance corresponds to the capacitance that is obtained by a series connection of the oxide capacitance and the capacitance across the surface depletion region:

$$C' = \frac{1}{1/C'_{ox} + x_d/\varepsilon_s} \qquad (2.11)$$

where x_d is the width of the surface depletion layer, which depends upon gate bias as well as the doping and the oxide properties. From above equation we see that the capacitance of the system decreases as the depletion region widens.

When the gate bias is increased sufficiently to invert the surface, a new feature must be considered to describe the MOS capacitance behavior. We recall

The requirement of pattern generation in displays, using photolithography, needs chemical etchability of the film. These factors make Sn doped In_2O_3 films as the most suited transparent conductor for displays. Windshield heaters and front surface infra-red reflectors require excellent chemical and mechanical resistance making SnO_2 as the best material for this purpose. Active applications like gas sensors, thin film resistors, electronic devices, etc. require a detailed knowledge of various optical, electrical, structural and chemical properties of transparent conductors. The requirement for electronic devices becomes very complicated. In addition to high transparency and low sheet resistance, the transparent conductor should form a high barrier with semiconductors like silicon. Both SnO_2 and In_2O_3 films, deposited by spray hydrolysis, have been found to give high barriers with n-type silicon, resulting in solar cells with more than 14% efficiencies [5]. Excess diode currents in these devices, however, result in comparatively poor fill factors, and the efficiencies are limited by the fill factors. The carrier transport processes across the barriers, and the role of traps produced by deposition processes in governing the transport processes, become very important. In addition to traps, the deposition processes are expected to affect the interface state distribution at $Si-SiO_2$ interface, which governs the performance of TCOS structure based devices like

solid state imaging devices. Therefore, properties of transparent conductors, especially those which affect the interface, become very important, and transparent conductor materials and processes require evaluation from entirely a different angle .

We have chosen to study interface defects in transparent conductor-silicon surface barrier devices prepared by different techniques of film deposition. The emphasis was on depositing good quality transparent conducting films, so that surface barrier devices could be fabricated, and interface defects could be studied. We have not tried to carry out a systematic study of variation in film properties with deposition parameters.

Chemical vapor deposition (CVD) was selected as chemical process for film deposition, since it is generally expected to yield more uniform and reproducible films compared to spray hydrolysis, making it more suitable for sophisticated electronic devices. We have chosen to deposit films using hydrolysis of chlorides since in that case the reagents and reactions used become same as those used in spray hydrolysis. The results on the study of traps in chemical vapor deposited samples could, therefore, yield results equally useful for spray deposited devices. Another reason for selecting chemical vapor deposition process was that its use in fabrication of

surface barrier devices, either heterojunction or TCOS structure, is hardly explored. Films of SnO_2 and Sb doped SnO_2 have been deposited by chemical vapor deposition. The reason for selecting SnO_2 based films is that chlorides of tin are considerably cheap compared to chlorides of indium, and hence deposition of SnO_2 films (undoped and doped) by hydrolysis is quite extensively used for various applications, including solar cells. The films have been deposited on polished silicon and polished fused silica substrates. The transmittance as a function of incident photon wave length, and sheet resistance (and resistivity) of these films have been measured. The transmittance data are used to determine the band gap. Electron microscopic investigations have been carried out to determine the grain size while X-ray diffraction has been used to identify various phases present in the film. All these characterizations were done to assess the quality of transparent conducting films. X-ray investigation was thought useful to identify various phases and compounds in the film which could throw some light on the chemical origin of interface defects.

Deposition of transparent conductors by physical process, like sputtering, has been extensively used for sophisticated applications like electronic devices [1,2]. Electron beam evaporation has also been used to deposit transparent conducting films, especially for solar cells, but its application in other surface barrier devices is relatively unexplored. The physical processes, like

sputtering and electron beam evaporation, involve interaction with charged particles. The SiO_2 film and Si-SiO_2 interface in electronic devices encounter radiation damages due to their interaction with ions, electrons and photons (X-rays). The study of damage in TCOS structures prepared by physical deposition processes becomes very important. Since the nature of damage is mostly same in sputtering or e-beam evaporation, the results will have bearing on both the processes. Reactive sputtering from metal targets, usually requires post deposition annealing in either oxidizing [6] or reducing [7] ambient, depending on initial sputter conditions, to obtain good quality transparent conducting films. The control of film stoichiometry has been found to be relatively easier in case of sputtering from oxide targets but problems like contamination from hot pressed targets, excessive heating of target during deposition, etc. are frequently encountered [1]. Highly transparent and conducting films of Sn doped In_2O_3 have been reported to be easily deposited by direct evaporation from oxide source [8]. Introduction of sufficient amount of oxygen during deposition has been found to eliminate the requirement of post deposition heat treatment [9]. We have therefore decided to study the damage in electron beam deposited Sb doped In_2O_3-SiO_x-Si surface barrier devices. The deposition of films has been carried out under residual gas atmosphere and under oxygen partial pressure. Post deposition heat treatment in residual

gas atmosphere, in inert atmosphere, and under oxidizing as well as reducing ambients have been tried. The detailed characterization of the films has not been carried out. Only annealing effects have been studied. Sufficiently transparent and conducting films have been deposited by this method and TCOS structures have been fabricated to study the interface damage .

2.2 METHODS OF DEPOSITION AND PROPERTIES OF TRANSPARENT CONDUCTING FILMS

2.2.1 Film Deposition Techniques

Transparent conducting films have been deposited by various methods which can be broadly classified as : evaporation, sputtering, reactive ion plating, chemical vapor deposition, spray hydrolysis and miscellaneous techniques. These have been reviewed by Vossen [1] and Chopra et al [2], and are summarised below.

Evaporation

Evaporation is a common technique for metal film deposition. Post oxidation of evaporated films has been employed to prepare thin films of transparent conductors such as SnO_2, In_2O_3 and ZnO. The transparency and conductivity are governed by oxidation temperature. The process suffers the drawback of the possibility of incomplete oxidation of thicker films [10].

Reactive evaporation of Sn, In and Sn-In alloy, in oxygen atmosphere, has been used to deposit SnO_2, In_2O_3 and Sn doped In_2O_3 films. The resistivity strongly depends on oxygen partial pressure and reduces as the oxygen partial pressure is increased to 10^{-4} Torr after which the resistivity starts increasing [11]. Higher substrate temperatures result in better crystallinity with increase in mobility [11].

When thermionically assisted plasma is established during reactive evaporation to activate the reaction, the process is generally called activated reactive evaporation (ARE). Excellent quality transparent conducting films of Sn doped In_2O_3, Sb doped SnO_2 and ZnO have been deposited by this method [11-14].

Direct evaporation of SnO_2, In_2O_3, Sn doped In_2O_3 and ZnO has been carried out using thermal [9,15], electron beam [8,16] and flash evaporation [17]. SnO_2 cannot be evaporated thermally due to its high melting point and electron beam evaporation is normally employed. As deposited films generally have low transmittance and high resistivity since the oxides normally reduce to form films of lower oxides during evaporation. Transmittance and conductivity can be improved either by post oxidation of films [15], or by introducing oxygen during evaporation [9]. The final electrical and optical properties of the films, in case of post deposition oxidation, are determined by the extent of diffusion controlled oxidation of less oxidized species. Substrate temperature and oxygen

partial pressure are the main control parameters in case of oxidation during deposition. Though substrate temperature of about 400°C is generally used during direct evaporation highly transparent and conducting films of Sn doped In_2O_3 have been reported by electron beam deposition on substrates at 150-200°C [8]. The dependence of resistivity and transmission on substrate temperature and subsequent oxidation temperature has also been studied for Sn doped In_2O_3 films [15]. Thus higher oxygen partial pressure (sufficient to oxidize all suboxide species), adequate substrate temperatures, and fast deposition rates (to suppress the dissociation of oxides) are expected to give better quality transparent conducting films [2].

Sputtering

Various forms of sputtering like d.c., r.f., magnetron, and ion beam sputtering, have been used to deposit transparent conductors. As in case of evaporation, the sputtering also can either be reactive, i.e., sputtering from metallic targets in oxidizing atmosphere, or direct sputtering from oxide targets. Sputtering rates are more easily controlled than evaporation rates. Also sputtering is more directional than evaporation, and expensive source material is less wasted. However, sputtering is slower and more complicated than evaporation and hence special care is to be exercised.

Thin films of CdO, SnO_2, Sb doped SnO_2, In_2O_3, Sn doped In_2O_3, and Cd_2SnO_4 have been deposited by reactive sputtering [6,7,18,19]. As sputtered films are usually amorphous if deposited on unheated substrates, elevated substrate temperatur or post deposition heat treatment result in polycrystalline films. As sputtered films generally have high resistivity and normally require post deposition high temperature heat treatment in either oxidizing [6] or reducing [7] ambient depending on initial sputtering conditions. Typical deposition rates for reactive sputtering are 50 Å - 300 Å min^{-1}.

Sputtering from oxide targets normally result in better control of film stoichiometry and the need for post deposition high temperature annealing is minimized. However, target fabrication is quite difficult. Hot pressed targets are generally porous resulting in inexhaustible sources of contamination [20]. Another problem associated with oxide targets is excessive target heating requiring very efficient cooling [1]. Target mounting therefore becomes very critical. Highly transparent and conducting films of SnO_2 [21], Sb doped SnO_2 [22], In_2O_3 [23], Sn doped In_2O_3 [24-26], ZnO [27], and Cd_2SnO_4 [28] have been deposited by sputtering from oxide targets. Optimum value of substrate temperature obtained by various workers varies from 150 to 500°C. Addition of oxygen in the sputtering gas (Ar) over a very narrow range of pressure

has been found to significantly improve crystallinity, mobility, transmittance and IR reflectance of these films [24,25]. Typical deposition rates for sputtering from oxide targets are 100 Å - 200 Å min^{-1} [24].

Ion beam sputtering from oxide targets, at substrates temperatures as low as 80°C, has been employed to deposit very good quality Sn doped In_2O_3 films [29]. It has also been used to deposit SnO_2 films [30]. The film properties are found to be dependent on oxygen partial pressure during sputtering [29].

Reactive Ion Plating

Reactive ion plating is basically reactive evaporation [31-33] or magnetron sputtering [32,34] of metals and alloys aided by a low power r.f. discharge (about 100 W) directed towards the substrate. It is a promising low temperature deposition technique. The bombardment of energetic ions provide energy to the surface of the substrate, and to that of the growing film, eliminating the need for substrate heating. Ionized reactive species also facilitate their reaction with evaporated or sputtered atoms. Transparent conducting films of In_2O_3 [32], Sn doped In_2O_3 [33,34], F doped In_2O_3 [31] and Cd_2SnO_4 [34] have been deposited by this method. The influence of various deposition parameters on the film properties havealso been studied in detail [32-34]. Typical deposition rates are 1000 Å min^{-1} for evaporation [33], and 100 Å - 500 Å min^{-1} for magnetron sputtering [34].

Chemical Vapor Deposition

Chemical vapor deposition is a simple, reproducible, and inexpensive process in terms of equipment cost, with the flexibility of introducing dopants easily when desired. The deposition can take place due to either pyrolytic or hydrolytic reaction. In pyrolytic process, the organometallic compounds thermally decompose at the heated substrate, and their insitu oxidation with C_2,H_2O or H_2O_2 results in the deposition of metallic oxide film. The hydrolytic process is based on the reaction of metal chlorides, with water vapor or oxygen, on the heated substrate. Doping is carried out by introducing suitable reactive species along with other reagents in the reaction chamber. Since all the reactive species are introduced in gaseous form, their concentration can be adjusted easily and desired stoichiometry obtained. Some basic reactions resulting in formation of SnO_2 by chemical vapor deposition are [2] :

$$SnCl_4(g) + O_2(g) \longrightarrow SnO_2(s) + 2Cl_2(g) \ ,$$

$$SnCl_4(g) + 2H_2O(g) \longrightarrow SnO_2(s) + 4HCl(g) \ ,$$

$$(CH_3)_4Sn(g) + 8O_2(g) \longrightarrow SnO_2(s) + 6H_2O(g) + 4CO_2(g) \ ,$$

where (g) stands for gaseous form and (s) stands for solid form. True reaction kinetics are very complicated which have been examined by Ghoshtagore [35]. The main process control

parameters in CVD are the gas flow, gas composition, substrate temperature and geometry of the deposition apparatus. High substrate temperatures increase deposition rate and favour anion vacancies, whereas low temperatures favour Cl^- incorporation in the films prepared by hydrolysis [36,37]. The amount of anion vacancies at any temperature is governed by the gas composition near substrate. The problem becomes more complicated for doped films. Since the equilibrium constants for the reactions of the host and dopant chlorides are usually different, and they vary with temperature in different ways, the ratio of dopant atoms to host atoms is not only different from that of the starting reagents, but it varies with deposition temperature [1]. Low deposition temperatures may lead to incomplete reaction resulting in undesired phases in the film, while high deposition temperatures give rise to contamination from the substrate. Substrate contamination becomes critical in case of alkali glass which introduce p-type dopants in SnO_2 and In_2O_3 films reducing their conductivity. Another problem with high substrate temperature is the possibility of preheating of gases by radiation, resulting in decomposition of reagents in gas phase rather than at substrate surface. Stagnation of gases around the substrate also results in similar problem. These may lead to a powder deposit instead of a smooth film or the film prepared may be hazy [38]. System geometry and gas flow therefore play a vital role in

determining the uniformity and quality of films deposited by chemical vapor deposition. All process parameters must be adjusted empirically at the beginning and then their proper control yields quite reproducible films. Each set up has its own set of optimized parameters which may not hold good for another set up. CVD is therefore more empirical in nature compared to other techniques.

Chemical vapor deposition has been used for deposition of SnO_2 [38-40], Sb doped SnO_2 [41], In_2O_3 [42], Sn doped In_2O_3 [43], and ZnO [42] films. Organometallic compounds suitable for deposition of In_2O_3 are uncommon and expensive, but those used for SnO_2 are inexpensive. SnO_2 has been deposited by both the pyrolytic [38,41] as well as the hydrolytic [36,39,40] reactions. ZnO film has been deposited by pyrolytic process [42].

Substrate temperatures around 400°C have been commonly employed. Low substrate temperatures (< 350°C) have been reported to result in amorphous films, but higher temperatures favoured larger grains, better crystallinity and higher mobility [39]. Typical deposition rates are 300 - 1000 Å min^{-1}; but a continuous CVD set up has been reported for deposition of SnO_2 films on moving glass substrate, with deposition rates of 1 micron sec^{-1}, producing films of 80% transmittance, and 3×10^{-4} Ohm.cm resistivity [40].

Spray Hydrolysis

Spray hydrolysis process has been developed mainly for large area film deposition at relatively low cost. The process involves spraying of an aqueous solution containing soluble metallic compounds on a heated substrate. The basic reaction involved is same as that mentioned in chemical vapor deposition. The liquid droplets may vaporise before reaching the substrate or react on it after splashing. Splashing of liquid droplets is not desired since it gives a thermal shock to the substrate and results in nonuniform film. This can be avoided either by preheating the droplets to vaporise [44] or by using an inverted arrangement [45].

Spray hydrolysis has been extensively used to deposit doped and undoped films of SnO_2 and In_2O_3. Undoped SnO_2 [44], Sb-doped SnO_2 [46] and F-doped SnO_2 films [45,47,48] have been deposited by spraying alcoholic solutions of $SnCl_4$ with $SbCl_3$, NH_4F, HF and trifluoroacitic acid as dopant sources. In_2O_3[49] and Sn doped In_2O_3 [47-49] films have been deposited using $InCl_3$ with $SnCl_4$ as the dopant source. Films of ZnO [50] and Cd_2SnO_4 [51] have also been deposited by this method. Addition of small quantity of HCl is reported to have improved the film quality [44,48,51].

Important control parameters are the substrate temperature solution composition, deposition time, nozzle to substrate distance and solution (gas) flow rates. Typical deposition temperatures are 450-550°C which result in polycrystalline films. Films grown at temperatures around 300°C are reported to be amorphous [44,48]. Increase in deposition temperature increases the grain size. Typical deposition rates are 1000 Å - 2000 Å min^{-1}. This method has many drawbacks making it unsuitable for sophisticated applications. A lot of starting material is wasted ($InCl_3$ is quite expensive). The substrate receives a thermal shock and the exact temperature during deposition is not known. The films produced are generally nonuniform and reproducibility is poor.

Miscellaneous Techniques

Many other techniques, which have not been mentioned above for deposition of transparent conducting films, are also being tried. These include dip technique, chemical solution growth, screen printing, glow discharge, and reactive triode sputtering [2]. The results on some of them are encouraging.

2.2.2 Properties of Transparent Conducting Films

The properties of transparent conducting films, prepared by various techniques, have been reviewed by several authors [1-4] These are summarised below.

Cadmium Oxide (CdO) : The electrical and optical properties of CdO were explored in detail in 1950s and have been reviewed by Haacke [3]. It is an n-type semiconductor with interstitial Cd providing free electron concentration in the range of 5×10^{16} to 1×10^{21} cm^{-3} depending on stoichiometric perfection. The fundamental optical absorption edge of CdO was found to exhibit a large shift from 2.3 eV to 2.7 eV as free carrier concentration increased. Single crystal with carrier concentration of 10^{19} cm^{-3} showed mobility as high as 300 cm^2 V^{-1} sec^{-1}, while thin films with carrier concentration of $10^{20} cm^{-3}$ showed mobility of about 120 cm^2 V^{-1} sec^{-1}. Best reported conductivity was 2×10^3 $mho.cm^{-1}$, while transmission at wavelengths longer than 5000 Å was in the range of 80 to 90% [3].

Two factors are responsible for CdO not receiving much attention for practical utilization [3]. Firstly, the transmission cutoff in high conductivity state ($E_g \sim 2.7$ eV) leads to absorption of blue light and the film appears greenish blue. More serious is the second factor of low resistance against atmospheric moisutre attack which excluded CdO from most of the applications.

Tin Oxide (SnO_2) : SnO_2 is the first and still the most widely used transparent conductor for commercial applications. It has acceptable electrical and optical properties, in addition to excellent chemical stability and mechanical hardness. Furthermore, it can be deposited by simple and inexpensive methods,like

spray hydrolysis, using low cost raw materials, although these may not yield the best film properties. SnO_2 has been investigated in great details, but films produced by different deposition techniques have normally resulted in widely varying properties.

SnO_2 is an n-type semiconductor with carrier concentration exceeding 10^{19} cm^{-3}. It has been deposited by practically all the techniques discussed earlier. The native defects giving rise to high conductivity have been identified as doubly ionized oxygen vacancies [52]. The oxygen ion vacancy concentration can be varied over a wide range by heat treatment [53,54]. SnO_2 films can be doped conveniently by Sb [55] and F[47] while Cl may contribute some free carriers in films prepared by hydrolysis [36]. Doping has been found to normally increase the conductivity by an order of magnitude. SnO_2 films (doped and undoped) have yielded conductivities in the range of 10^2 to 10^4 mho. cm^{-1} [2]. Other dopants like In,Te,W Cl,Br,I, etc. do not seem to affect conductivity significantly [2], though P [56] and As [57] have shown encouraging results.

SnO_2 retains its tetragonal structure in thin film form but shows preferred orientation with grain size between 200 - 600 Å, which depends on deposition temperature and doping [44,46]. SnO_2 film may contain additional phases like SnO, Sn_2O_3 etc. while Sb doping may result in phases like

Sb_2O_4. These secondary phases can alter the electrical and optical properties of SnO_2 films. For example, SnO may reduce transmittance due to its smaller band gap. It may also increase the film resistivity. Dopants like Sb have also been found to reduce transmittance but F does not affect it [46].

Energy band investigations for SnO_2 indicate multiplicity of non-parabolic conduction and valence bands resulting in both direct and indirect optical transitions [58,59]. Various investigators have reported direct optical band gap of 3.77 to 4.30 eV for undoped SnO_2 films [2,17] while the refractive index has been found to lie between 1.8 and 2.0 [2]. Antimony doping has been found to increase the optical bandgap slightly due to increase in carrier concentration [47].

The minimum reported sheet resistance is 8 Ohm/sq. for a 6000 Å thick F-doped film. It had an average transmittance of 80% for visible light and mobility was 23 $cm^2V^{-1}sec^{-1}$ [47]. The highest reported mobility is 46 $cm^2V^{-1}sec^{-1}$ for a F-doped SnO_2 film with sheet resistance of 8.6 Ohm/sq [60]. The lowest reported resistivity is $3x10^{-5}$ Ohm-cm for Sb-doped SnO_2 film prepared by activated reactive evaporation [12].

Indium Oxide (In_2O_3) : Commercial utilization of In_2O_3 coatings began in 1970s with the need for substituting SnO_2 by some other transparent electrode in liquid crystal displays. Close tolerances in the flatness of the electrodes are essential

for liquid crystal displays which can best be achieved by the low temperature vacuum deposition processes like evaporation and sputtering. These processes were better established for deposition of In_2O_3 films. Another important factor was that In_2O_3 could be etched more easily than SnO_2 which facilitated a more economical photoetching procedure during manufacture of digital displays. In_2O_3 is also a superior transparent conductor compared to SnO_2 mainly because of higher mobility. Although chemically less resistant than SnO_2, its chemical stability is adequate for many applications.

The fundamental materials parameters of In_2O_3 are not as well established as those of SnO_2. This is because In_2O_3 single crystals of quality comparable to the best SnO_2 crystals have not been prepared so far [3]. Undoped In_2O_3 films have been found to exhibit a direct optical bandgap which lies between 3.55 to 3.75 eV and increases with increasing carrier concentration [7,61,62]. The native defect responsible for n-type conduction in undoped films has been identified as interstitial indium ions [63].

In_2O_3 films are generally polycrystalline with cubic structure [7,23]. Reactively sputtered films have a typical grain size of about 100 Å [7] while films prepared by various techniques show a <100> or <111> preferred orientation [23]. Films deposited by various techniques have resulted in mobilities in the range of 10-75 $cm^2V^{-1}sec^{-1}$, carrier concentration

around 10^{19}-10^{20} cm^{-3} and resistivity ~ 10^{-3} Ohm-cm [1-4]. Heat treatment in reducing ambient has been found to improve the conductivity while that in oxidizing ambient decreased the conductivity [7]. The optical transmission in the visible region is generally about 75% - 90% [23], while the refractive index is reported to be between 1.9 and 2.08 [7,23].

The best values obtained for undoped In_2O_3 so far are mobility - 74 $cm^2V^{-1}sec^{-1}$, resistivity -$2x10^{-4}$ Ohm cm and transmittance -90%. These have been obtained by evaporating a mixture of In_2O_3 - 10 wt% In in an oxygen ambient [9], which incidently are the best values obtained for any undoped transparent conductor.

Sn doped In_2O_3 films (ITO films) retain the cubic structure of In_2O_3 with slight increase in lattice parameters. These films also exhibit a strong <100> or <111> orientation and typically the grain size varies between 400-600 Å [64]. Sn doped In_2O_3 films prepared by various techniques have resulted in carrier concentration of 10^{21} cm^{-3}, mobility in the range of 15-40 $cm^2V^{-1}sec^{-1}$, sheet resistance around 2-5 Ohm/sq, transmission about 90% and resistivity in the range of $7x10^{-5}$ to $5x10^{-4}$ Ohm cm [2]. Lowest reported sheet resistance is 1.6 Ohm/sq with transmittance of 73% [26].

Apart from Sn, the other dopants used in In_2O_3 films are Ti, Zr, Sb, Pb and F [31,49,65].F doped In_2O_3 films prepared by reactive ion plating have yielded $R_{sh} \sim 40$ Ohm/sq with $T \sim 80\%$ [31].

Cadmium Stannates (Cd_2SnO_4 and $CdSnO_3$) : Cadmium stannate is generally obtained in two phases, Cd_2SnO_4 and $CdSnO_3$. Both these phases have orthorhombic structure and are n-type semiconductors [3]. Their fundamental properties are mostly unknown but both show transparent conductor behaviour. Generally a film of cadmium stannate contains multiphases like CdO, Cd_2SnO_4, and $CdSnO_3$, but their relative amount depends on preparation conditions. The bandgap has been reported to vary from 2.06 to 2.85 eV depending on carrier concentration which is governed by deposition conditions [28].

Cd_2SnO_4 is very similar to In_2O_3 is electrical, optical, mechanical, and chemical properties, and both of them still have the highest reported solar transmission and infrared reflection Optimal properties have been obtained in films prepared by r.f. sputtering in oxygen and subjected to post deposition treatment [66]. Sheet resistance of 1 Ohm/sq with transmittance of 85% has been obtained in such films with thickness greater than one micron, while thin films of 1000-2000 Å have shown sheet resistance of about 15 Ohm/sq with transmittance of 87% [66].

$CdSnO_3$ is similar to SnO_2 in optical and electrical properties but mechanical and chemical properties are similar to Cd_2SnO_4. Highest reported conductivityfor $CdSnO_3$ is 1000 mho cm^{-1} compared to 6800 mho cm^{-1} in case of Cd_2SnO_4[67]. The transmission and infrared reflection of $CdSnO_3$ is also lower compared to equal thickness of Cd_2SnO_4 film.

Zinc Oxide (ZnO) : The electrical and optical properties of bulk ZnO have been studied extensively and reviewed [68]. Thin films of ZnO can be prepared by various techniques and can be doped. Undoped ZnO films retain bulk wurtzite structure and show strong c axis orientation, with grain size in the range of 50-300 Å [2]. Best undoped ZnO films have been obtained by activated reactive evaporation leading to resistivity in the range of 10^{-4} to 10^{-3} Ohm cm with transmittance ~ 90% [13]. Films obtained by CVD, spray pyrolysis, and r.f. magnetron sputtering have resulted in resistivity in the range of 10^{-3} to 10^{-2} Ohm cm with transmittance between 80 to 90% [2]. Indium and aluminium have been used as dopants for films prepared by spray pyrolysis and Indium doped film has resulted in carrier concentration of 5×10^{20} cm^{-3}, mobility of 15 $cm^2V^{-1}sec^{-1}$, resistivity around 8×10^{-4} Ohm cm and transmittance around 80% with sheet resistance in the range of 10-15 Ohm/sq [2].

2.3 EXPERIMENTAL DETAILS

2.3.1 Chemical Vapor Deposition of SnO_2 and Sb Doped SnO_2 Films

The Chemical Vapor Deposition Setup

Figure 2.1 illustrates the experimental setup used for chemical vapor deposition of SnO_2 films. It consisted of a 1000 mm long furnace tube of 45 mm diameter (outer) placed inside a 900 mm long resistance heated furnace. Both the ends of the furnace tube had detachable seals. The inlet seal contained one 8 mm diameter thermocouple tube sealed at one end, and three 6 mm diameter tubes for gas connections, which had their openings approximately 10 mm, 30 mm and 60 mm away from inlet seal into the furnace tube. Each of these three tubes was connected to a bubbler used for keeping deionized water, Sn source, and Sb source, respectively. The bubblers used for keeping Sn source and Sb source were immersed in a water bath whose temperature could be controlled, while deionized water was kept at room temperature. The carrier gas flow through deionized water could be controlled from 0-5000 cc/min, while that through Sn and Sb sources could be controlled from 0-1500 cc/min and 0-40 cc/min, respectively. A chromel-alumel thermocuple was inserted through the thermocouple tube at inlet seal, and was placed close to substrate position to measure the temperature during deposition. The exhaust seal contained a

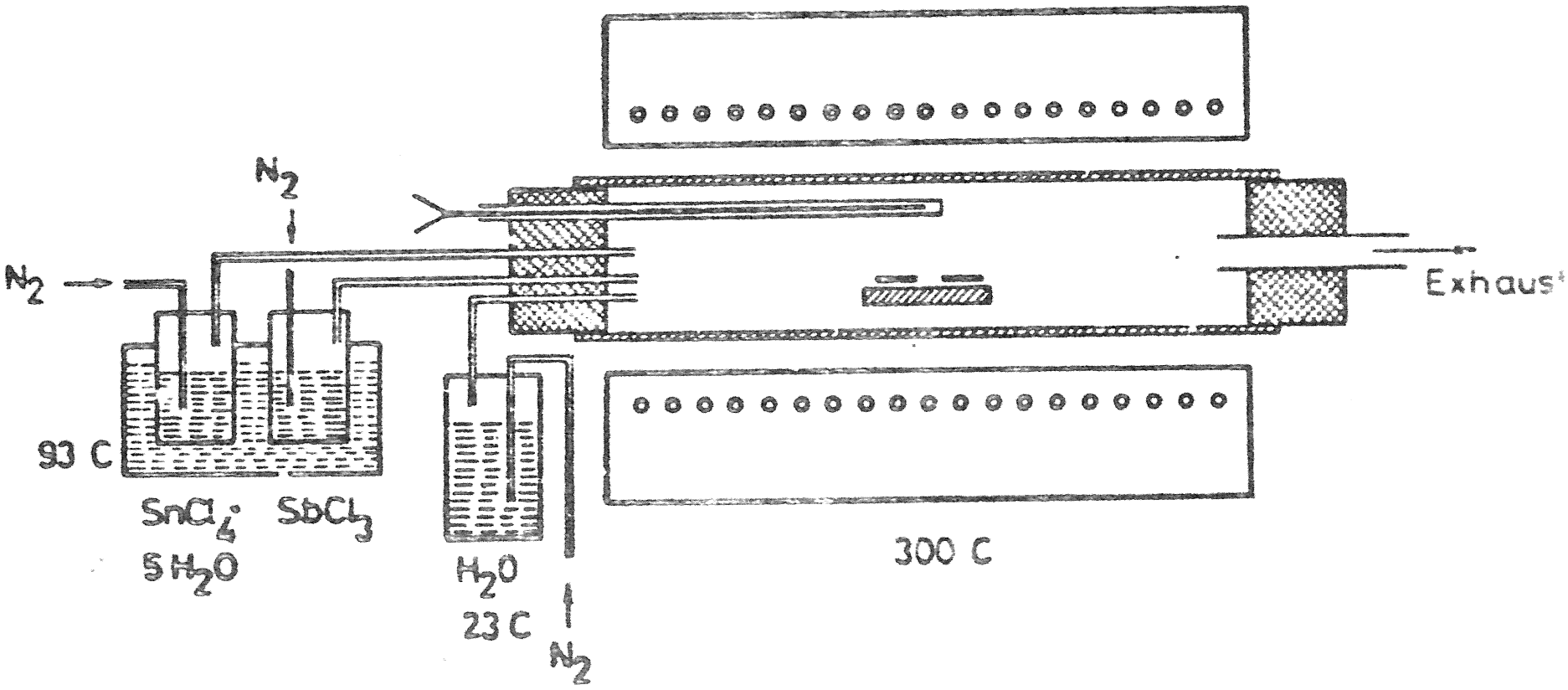


Figure 2.1 Schematic of the set-up used for chemical vapor deposition of undoped and Sb doped films of SnO_2

a 22 mm diameter tube connected to another container, where hot gases could be cooled before being exhausted out of the room through a PVC tube connected to main exhaust duct.

The substrates were kept horizontally on the boat, mainly to facilitate masking. Thin molybdenum (5 mils thick) masks having 2.0 and 3.0 mm diameter were employed to define areas of the surface barrier devices, while thin molybdenum strips were used to form steps in large area samples to enable thickness measurements. Exhaust end of the furnace tube was used for introducing samples into the furnace.

Analysed reagent grade $SnCl_4.5H_2O$, and $SbCl_3$ were used as sources for Sn, and Sb (dopant), respectively. Deionized water of 12-14 M Ohm-cm was used as oxidizing agent. Nitrogen was used as the carrier gas. Polished silicon wafers and polished fused silica pieces were used as the substrates. Separate reagent transfer spoons were used for handling Sn and Sb sources.

All the parts like furnace tube, gas inlet tubes, thermocouple tube, exhaust tube, bubblers, exhaust container and reagent transfer spoons were thoroughly cleaned using hot solvents initially. These were then etched in diluted HF and rinsed in deionized water. The flexible tubes for gas connection at the inlet end and at the exhaust end were cleaned with methanol. Though the same furnace was used during

all the experiments, different sets of furnace tubes, end seals, and other attachements including boats, masks etc. were used for deposition of undoped and Sb doped SnO_2 films. These were also replaced periodically to minimize the effect of earlier deposits on the film properties.

Establishment of Deposition Parameters

Initial deposition runs were carried out with a solution of $SnCl_4 \cdot 5H_2O$ in deionized water as the source for deposition. The solution was made by dissolving 25g $SnCl_4 \cdot 5H_2O$ in 10 CC deionized water. Furnace was heated to 400°C with 40 CC/min N_2 flowing through it. The substrates were degreased in warm solvents and loaded on a boat making different angles to the direction of gas flow. The boat was placed at the centre of the furnace. The solution was heated in the bubbler till it started boiling. The carrier gas flow through the solution was varied between 250-550 cc/min, and the deposition time was varied between 15-40 min. Although a few good films were obtained, the films deposited in this manner were nonuniform in thickness and had whitish haze. They even had whitish translucent deposits at times. The possible reasons for non-uniformity were that the solution concentration and temperature were not property controlled. The solution concentration varied during the course of deposition which was indicated by the change in viscosity of the solution. The reason for whitish haze or deposit was that reagent vapors were reacting

in vapor phase before reaching the substrate due to their sufficient preheating, as was observed by Tabata et al. [38]. The furnace tube also showed some regions of transparent films with bright interference colours, closer to the gas inlet end, while the remaining regions showed either no deposit or whitish translucent deposit. This confirmed that the reaction was taking place before the vapors reached the heated substrate. Based on this preliminary investigation, it was decided to use separate bubblers for $SnCl_4$ and deionized water, control their temperatures separately, place the substrates in the region where good films were obtained on the furnace tube, and lower the deposition temperature to avoid undesired pre-heating of the vapors.

In subsequent deposition runs to establish the process parameters, $SnCl_4.5H_2O$ was kept in a bubbler which was immersed in a water bath with temperature controller. Temperature of the water bath was measured by a thermometer. $SnCl_4.5H_2O$ melted around 70°C. After a few trial runs with molten $SnCl_4$ temperature between 70°C and 98°C, it was decided to keep the temperature of water bath at 93°C. This helped in minimizing the rate of depletion of water level from the bath, and at the same time developed enough vapor pressure of $SnCl_4$ to enable its transportation into the furnace in sufficient amount. Deionized water bubbler was also kept in hot water bath during a few initial deposition runs, but was later on maintained at

room temperature (23°C). The furnace was heated to 400°C with N_2 gas bubbling through deionized water at a rate of 50 cc/min in case of bubbler kept at 93°C, or 1250 cc/min in case of bubbler kept at 23°C. A 100 mm long glass rod of 8 mm diameter, degreased in warm solvents, etched in HF, and rinsed in deionized water, was introduced into the furnace. The deposition was carried out with N_2 gas flow rate through molten $SnCl_4$ as 550 cc/min. Deposition time was 60 min. Faint fumes were observed in the exhaust chamber throughout deposition. The glass rod showed film with bright interference colours in certain regions closer to gas inlet end. The temperature at various places in the furnace was measured with the help of thermocouple. It was observed that good films were deposited in the region having temperature between 275-375°C. The experiment was repeated many times and the outcome was reproducible. A few deposition runs were then made using silica substrates kept on a boat in the above-mentioned temperature region. Good transparent conducting films were deposited each time on the substrates. The inclination of the substrates, and marginal changes in gas flow rates through molten $SnCl_4$ and deionized water did not affect the film quality appreciably. Finally it was decided to establish the typical deposition parameters as follows :

Substrate position - 16 cm from $SnCl_4$ vapor entry point in the furnace

Substrate temperature - 300°C

Substrate inclination - horizontally flat, essentially to facilitate masking

Temperature of molten $SnCl_4$ - 93°C

Temperature of deionized water - 23°C

N_2 bubbling rate through molten $SnCl_4$ - 550 cc/min

N_2 bubbling rate through deionized water - 1250 cc/min

Deposition time - 60 min

Doping with Sb was tried with $SbCl_3$ kept in another bubbler and maintained at 93°C. The gas flow rate through molten $SbCl_3$ was varied between 0 - 40 cc/min, while other deposition conditions remained same as mentioned above. This yielded good quality Sb-doped SnO_2 films.

Deposition of SnO_2 films

SnO_2 films for electrical and structural characterization were deposited mainly on silicon substrates. Polished fused silica substrates were used for optical characterization.

The substrates were degreased in warm trichloroethylene, in warm acetone, ultrasonically cleaned in acetone and finally degreased in warm methanol. Subsequently the substrates were etched in HF and rinsed in deionized water having a resistivity of 12-14 M Ohm cm. Two sets of fused silica boats and

molybdenum masks (one set each for undoped and Sb doped films) were also degreased in above mentioned manner. The boats were also etched in HF and rinsed in deionized water.

Fresh charges of deionized water, $SnCl_4.5H_2O$, and $SbCl_3$ (whenever doping was needed) were used during each deposition runs. Separate sets of furnace tube, attachments, boat, and masks were used for undoped and Sb SnO_2 film deposition as mentioned earlier.

The furnace was brought to the required temperature with only N_2 gas flowing through deionized water. Water bath temperature was raised to 93°C and was controlled. The substrates were loaded horizontally on the boat with appropriate masks (if any), and placed in the furnace tube at about 16 cm from $SnCl_4$ vapor entry point. The substrate temperature was held at about 300°C and monitored with the help of thermocouple. N_2 flow rates through $SnCl_4$, $SbCl_3$ and deionized water were adjusted as standardized and mentioned earlier. Flow of N_2 through $SnCl_4$ and $SbCl_3$ bubblers were activated only after positioning the substrates at proper place, and sealing the furnace tube with exhaust seal. The inlet gas connections were such that N_2 bubbling through deionized water, $SnCl_4$, and $SbCl_3$ was introduced into the furnace at about 10 mm, 30 mm, and 60 mm away from the inlet seal, respectively. Faint fumes were observed in the exhaust chamber throughout the deposition which was an indication that deposition at uniform rate was in

progress. The amount of fumes observed was more during deposition of Sb-doped films. Molybdenum strips were used as masks to form steps in the films deposited in case of samples made for sheet resistivity and subsequent thickness measurements. The samples for optical, X-ray, and transmission electron microscopic investigations had no step in the film.

2.3.2 Electron Beam Deposition of Sn doped In_2O_3 Films

The Evaporation Setup

Electron beam evaporation of Sn doped In_2O_3 was carried out in Varian Model 112B ultrahigh vacuum system with 12 inch diameter belljar. This vacuum system employs two liquid nitrogen cooled sorption pumps as the roughing pumps to evaluate the chamber from atmospheric pressure to less than $1x10^{-3}$ torr pressure. The system is pumped with one sorption pump upto about 1-2 torr pressure which is then sealed and the other sorption pump is activated to bring down the pressure to less than $1x10^{-3}$ torr pressure. The system is evaluated further with the help of triode ion pumps which, together with titanium sublimation pump fitted in the system, can bring down system pressure to about $2x10^{-11}$ torr, if stainless steel chamber is used and adequate baking carried out. With a glass belljar, pressure up to about $2x10^{-9}$ torr could be obtained, though pressure upto $1x10^{-7}$ torr could be obtained easily in a reasonably short time (approximately 40 min). A liquid nitrogen cooled cryopanel is employed to cool the surface around titanium sublimation pump which

improves the pumping rate. Chamber pressure from 1.0 to $1x10^{-3}$ torr is read by thermocouple gauge while dual filament ionization gauge reads chamber pressure from 10^{-4} torr to $2x10^{-11}$ torr. The triode ion pumps also give pressure in the pump region since the current in ion pumps depends on the gas pressure. The triode ion pump control unit has provision for measuring the pressure or the current. A pressure interlock is provided in triode ion pump control unit which switches off if pressure exceeds $1x10^{-5}$ torr.

The evaporation source employed was Varian Three Crucible 2 kW E-Gun and the power was controlled with the help of E-Gun Source Control Unit. The electron gun control unit is current regulated and minor changes in line voltages do not affect the beam power. The line voltage to the vacuum system and e-gun control unit was regulated with the help of a voltage regulator. The e-gun contains a tungsten filament as the electron source. The electrons are confined to a narrow beam and directed towards the target with the help of magnetic focussing. Single filament is used as the electron source while the position of crucible can be changed from outside to bring the desired crucible to electron path. The beam voltage is 4 kV and the beam current can be varied from 0-500 mA. Maximum power of e-gun source is 2 kW. The tungsten filament is fed with a voltage in the range of 0-6V ac resulting in 0-25A current through filament. The crucible is cooled with the help of recirculating chilled water flowing at a rate of about 1.9 litres/min. The e-gun source operates in a pressure

range of 5×10^{-4} torr - 10^{-11} torr and a pressure interlock switches the e-gun power supply off if the chamber pressure exceeds about 1×10^{-4} torr pressure. Maximum volume of evaporant that can be charged in one crucible is 1.1 cc. The position of crucible can be moved to uniformly evaporate the evaporant from all regions avoiding excess evaporation from one region, which might result in a hole drilled in evaporant at that place. The emission current is displayed on a 0-500 mA ammeter on the source control unit and the beam power can be found by multiplying the output voltage of 4KV dc to emission current. The source control unit has a provision for setting an upper limit to emission current and the e-gun supply is switched off as soon as the upper limit is crossed. A hand held potentiometer can be used as remote control to adjust e-beam power.

The arrangement for substrate mounting inside the vacuum chamber is shown in Figure 2.2. A stainless steel substrate plate is mounted on a tripot stand in the chamber so that the distance between the source and the substrate is about 17 cm. The substrate plate has suitable grooves to hold substrate holders. The substrate holders are made of copper to enable proper heating of the substrate. The substrates are kept on suitable thin copper masks in side the grooves made in substrate holder to avoid their displacement during evaporation. Copper discs are kept on the substrates to enable their uniform

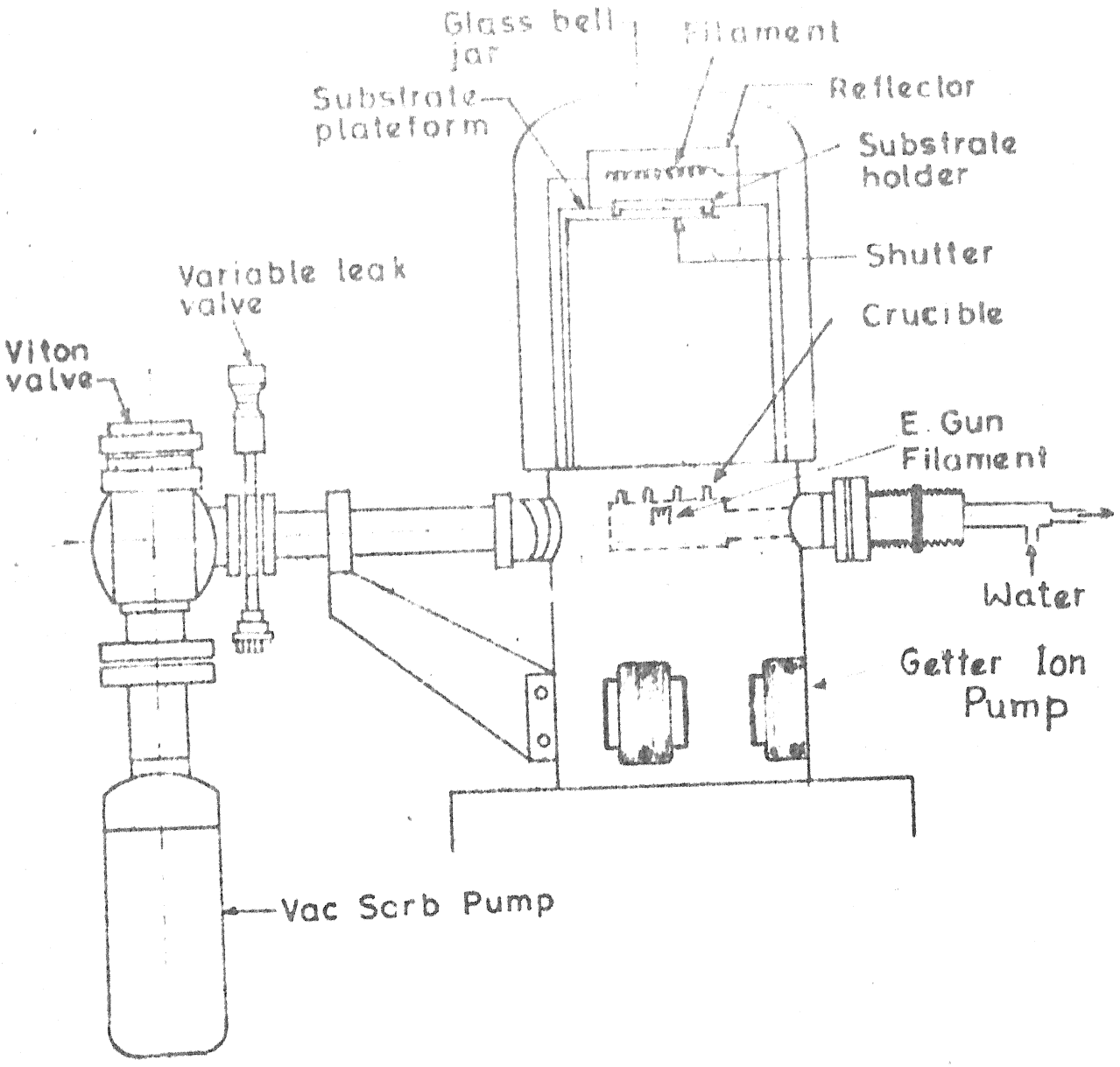


Figure 2.2 Schematic of the set-up used for e-beam deposition of Sn doped In_2O_3 films

heating. The substrates can be heated with the help of a resistance heated filament placed close to the back side of the substrates. A stainless steel radiation shield is kept close to the filament to achieve more effective heating of substrate, and to avoid heating of other parts including glass belljar. A chromel-alumel thermocouple is fixed to the substrate holder to monitor the substrate temperature. A stainless steel shutter fixed to a rotary motion feed through is employed to mask the substrates from deposition of material when ever not desired.

Deposition of Film

Silicon wafers and polished fused silica substrates were used for deposition of Sb doped In_2O_3 films by e-beam evaporation. The substrates were degreased and etched in the same way as discussed earlier for chemical vapor deposition of SnO_2 films. Hot pressed In_2O_3:SnO_2 (91:9 mole percent) tablets from Atomergic Corp., USA were used as the evaporant. These tablets were degreased in warm solvents and loaded on the e-gun crucible. All the attachments inside the vacuum chamber, like shutter, substrate plate, heating filament, masks, substrate holders etc. were thoroughly degreased in warm solvent before introducing into the chamber. The substrates were kept on suitable masks inside substrate holder groves and the substrate holders were mounted on the substrate

plate at desired locations. The shutter was brought between the source and the substrate. The system was evacuated to a pressure less than $1x10^{-7}$ torr. Chilled water was recirculated through the e-gun crucible. The cryopanel was chilled with liquid nitrogen, if desired. The substrates were heated to desired temperature and the temperature was monitored with the help of thermocouple and digital multimeter. The substrate temperature was allowed to stabilise before deposition was carried out. The electron beam power was increased slowly till significant evaporation began. Hand held potentiometer was employed for adjusting e-beam power. After initial heating and evaporation from evaporant, the shutter was moved to allow deposition on substrates through mask. The evaporation was carried out either in residual gas atmosphere or in oxygen partial pressure. Oxygen was introduced in the chamber in a controlled way through a finely adjustable leak value, if desired. Typical oxygen partial pressure, was $1x10^{-5}$ torr. Typical deposition time was 60 min and the pressure during deposition was around $1x10^{-5}$ torr. The substrates were generally kept at 300°C temperature, though some depositions were carried out with substrates kept at room temperature.

Post Deposition Annealing of Films

The deposited films were subjected to various post-deposition annealings to evaluate their effect on film properties. The annealings were carried out in vacuum, in residual

air, in oxygen partial pressure, and in hydrogen partial pressure. Annealings were also carried out in standard tube furnace in inert, oxidizing, and reducing atmosphere. The annealing temperatures varied from 300--550°C and the durations varied from 30 min to 60 min, though the same sample was subjected to many annealing cycles.

2.3.3 Characterization of SnO_2 Films

Electrical Characterization

The sheet resistance of SnO_2 films deposited on polished fused silica and silicon substrates were measured using Keithley Model 530 Type All System. Four point probe measurement method with appropriate correction factor for the size of the sample was used for this purpose [69]. The sheet resistance R_{sh} is given by :

$$R_{sh} = 4.53 \frac{V}{I} F \qquad (2.3)$$

where V is the voltage developed across inner probes, while I is the current flowing through outer probes. F is the correction factor for sample size.

The conductivity type was measured using hot and cold probe method. The thickness of the film having a step was measured using Varian Å-scope interferometer. Initially aluminum was evaporated on one sample to get a reflecting surface in the region where step is formed on the sample.

Though aluminum film on bare substrate had very good reflectance, it had poor reflectance on SnO_2 film making it unsuitable for thickness measurement by interferometer. Later silver and gold films were tried for this purpose. Though both of them gave good reflectance on SnO_2 film as well as on bare substrate, silver had better reflectance on SnO_2 film and hence was used on all the films for this purpose. The film thickness, t, using interferometer is given by :

$$t = \frac{\text{fringe offset}}{\text{fringe spacing}} \cdot \lambda/2 \quad , \qquad (2.4)$$

where λ is the wavelength of the light source used. In Varian Å-scope interferometer, the light source is sodium lamp and hence λ = 5892 Å.

The volume resistivity of the film was calculated using Equation (2.1), i.e., $\rho = R_{sh} \cdot t$.

Optical Characterization

Average visible light transmission measurement was used as a rough estimate for transmission of undoped SnO_2 films deposited on glass substrates. A calibrated standard solar cell was used as the light sensor, a tungsten bulb was used as the light source. The short-circuit current of the solar cell was measured with a bare substrate covering its surface. The reference substrate was similar to the one used for film deposition. Care was taken to ensure that no light reached the

where A and B are constants, and $h\nu$ is the energy of incident radiation. When $h\nu = E_g$, then $\alpha_\lambda = 0$. Equation (2.6) shows that a plot of $(\alpha_\lambda)^{1/B}$ vs $h\nu$ should be a straight line, with intercept at $\alpha_\lambda = 0$ giving the bandgap of the material. Combining Equations (2.5b) and (2.6), we find that if $[\ln(1/T_\lambda)]^{1/B}$ for any film is plotted as a function of incident energy, the intercept at $\ln(1/T_\lambda) = 0$ will give band gap. B has to be calculated by trial and error so that a straight line is obtained. B has a value of 1/2 for direct transition and 3/2 for indirect transition [70]. For some cases it has also been found to give a value of 1 or 2.

Structural Characterization

Identification of various phases of tin oxide and antimony oxide (if any) in the SnO_2 films deposited on large area silicon substrates was done by X-ray diffraction analysis. A Rich Seifert Isodebyeflex 2002 X-ray diffractometer was used for this purpose. CuK_α radiation ($\lambda = 1.54$ Å) was employed and the magnitude of diffraction peaks and angle of incidence (θ) were recorded. The 'd' values corresponding to various peaks were calculated using Braggs relation $2d\sin\theta = n\lambda$. The calculated 'd' values were matched with standard 'd' values from the literature [71] to identify the phase giving rise to the particular peak.

Tin oxide films deposited on silicon substrates were also examined under a Philips EM 301 transmission electron microscope for this purpose. SnO_2 layers were stripped from the silicon substrate by etching the substrate in a mixture of HF and HNO_3 followed by decanting of the unetched film in deionized water. These films were then supported on copper grids. Electron micrographs as well as electron diffraction patterns were recorded on photographic plates. The micrographs were used to calculate the average grain size in the film while the diffraction pattern indicated the crystallinity of the film.

2.3.4 Characterization of In_2O_3 Films

Detailed characterization of e-beam deposited In_2O_3 films has not been carried out. The sheet resistance of as-deposited and annealed films have been measured. Visual inspection of transmittance of films deposited on fused silica substrates, and reflectance and brightness of interference colours of films deposited on silicon substrates, have been used as guidelines for assessing the suitability of films for fabricating surface barrier devices.

2.4 RESULTS AND DISCUSSION

2.4.1 Properties of Chemical Vapor Deposited SnO_2 Films

Effect of Deposition Parameters : Initial trial deposition runs for undoped SnO_2 films were carried out with $SnCl_4$ and H_2O

sources kept at 93°C, and N_2 flow rates through them being 550 cc/min and 50 cc/min respectively. Initial SnO_2 films deposited on inclined substrates had nonuniform thickness which resulted in different interference colours on the same substrate. This probably was an indication of a large temperature gradient in the furnace tube along its radius. The interference colours, in case of films deposited on substrates kept horizontally on the boat, were uniform. Though different samples with different positions on the boat showed different interference colours, each substrate had uniform colour indicating uniform thickness over the whole area of the substrate. Moreover, masking of horizontally placed substrates was found easier, and hence the substrates were kept horizontally on the boad during subsequent depositions. Another feature observed was that the films deposited on substrates at temperatures around 300°C resulted in lower sheet resistance compared to films deposited at higher temperatures. The geometry of the deposition setup, rather than the substrate temperature, was probably responsible for this feature. The possible reason for this feature was that most of the reacting species had reacted earlier and deposited films on furnace tube before reaching the substrates. This was also supported by the fact that films deposited at higher temperatures had some hazy appearance while films deposited at about 300°C had bright

interference colours and good transparency. Undoped SnO_2 films deposited during trial runs resulted in sheet resistance in the range of 450-700 Ohm/sq for film thickness in the range of 900°-1400 Å. The deposition rate was found to vary between 16-25 Å/min. The resistivity of these films varied in the range of $(5-7)\times10^{-3}$ Ohm-cm, and average transmittance, measured with the help of a solar cell and tungsten lamp source, was found to be in the range of 85-90%.

Subsequently, during final deposition of undoped and Sb doped samples, $SbCl_3$ source was kept at 93°C and N_2 flow was varied between 0-40 cc/min, while H_2O source was kept at 23°C and N_2 flow was kept at 1250 cc/min. Table 2.1 summarises important deposition parameters and electrical properties of undoped as well as Sb doped SnO_2 films deposited on silica and silicon substrates. Undoped SnO_2 films deposited with water source at 23°C resulted in sheet resistance of 215-270 Ohm/sq compared to 450-700 Ohm/sq obtained for films deposited for about the same time with water source at 93°C. It was also found that increasing N_2 flow through $SnCl_4$ (93°C) and H_2O (23°C) to about twice the flow rates used during most deposition runs did not seem to alter the deposition rates or film properties appreciably. This can be seen from the properties of a few Sb doped films deposited with increased flow rates (cf. Table 2.1, samples CNT 11, CNT 12, CST 7, CST 8). Higher deposition rates at the same deposition temperature may

Table 2.1 : Summary of important deposition parameters and electrical properties of SnO_2 films prepared by chemical vapor deposition

Sl. No.	Sample No.	Subs. Temp (^oC)	Dep. time (min)	N_2 flow through $SbCl_3$ (cc/min)	R_{sh} (Ohm/sq)	t (Å)	ρ (Ohm-cm)	Dep. Rate (Å/min)
1	2	3	4	5	6	7	8	9
1.	CNT 0	310	45	-	250	-	-	-
2.	CNT 1	300	50	-	215	-	-	-
3.	CNT 2	300	50	-	270	-	-	-
4.	CNT 4	300	60	40	44	-	-	-
5.	CNT 5	300	60	14	100	-	-	-
6.	CST 1	315	60	40	185	-	-	-
7.	CNT 8	315	120	-	98	3000	2.9×10^{-3}	25
8.	CNOT 11	300	60	40	210	535	1.1×10^{-3}	9
9.	CNOT 12	300	60	28	300	-	-	-
10.	CNOT 13	300	60	40	185	720	1.3×10^{-3}	12
11.	CST 2	315	60	40	185	-	-	-
12.	CNOT 14	300	60	28	190	830	1.6×10^{-3}	14
13.	CST 3	315	60	28	175	-	-	-
14.	CNOT 16	300	60	28	270	620	1.7×10^{-3}	10
15.	CNOT 17	300	60	18	185	-	-	-
16.	CST 4	315	60	18	150	-	-	-
17.	CNOT 18	300	60	11	95	1840	1.7×10^{-3}	31
18.	CST 5	315	60	11	60	-	-	-

contd ...

1	2	3	4	5	6	7	8	9
19.	CNOT 19	300	60	11	60	1430	8.6×10^{-4}	24
20.	CNOT 20	300	60	11	75	-	-	-
21.	CNOT 21	300	60	6	160	-	-	-
22.	CNOT 22	300	60	6	175	1630	2.8×10^{-3}	27
23.	CNOT 23	300	60	40	160	1310	2.1×10^{-3}	22
24.	CNOT 24	300	60	40	205	-	-	-
25.	CNOT 25	300	60	-	180	-	-	-
26.	CST 6	315	60	-	135	-	-	-
27.	CNOT 26	300	60	11	265	980	2.6×10^{-3}	16
28.	CNOT 27	300	100	11	210	1200	2.5×10^{-3}	12
29.	CNOT 28	315	140	11	225	1850	4.1×10^{-3}	13
30.	CNOT 29	315	180	11	130	2495	3.3×10^{-3}	14
31.	CNOT 31	300	60	6	310	580	1.8×10^{-3}	10
32.	CNOT 33	300	60	18	175	1085	1.9×10^{-3}	18
33.	CNOT 34	300	60	23	175	860	1.5×10^{-3}	14
34.	CNOT 35	300	60	40	120	1300	1.6×10^{-3}	22
35.	CNOT 36	300	120	40	140	1480	2.1×10^{-3}	12
36.	CNOT 37	300	180	40	95	2120	2.0×10^{-3}	12

1	2	3	4	5	6	7	8	9
37.*	CNT 11	315	60	11	120	1225	1.5×10^{-3}	20
38.*	CNT 12	315	60	18	335	1050	3.5×10^{-3}	18
39.*	CST 7	315	60	40	290	-	-	-
40.*	CST 8	315	60	34	205	-	-	-

Note : i) The temperatures of $SnCl_4$ and $SbCl_3$ sources were 93°C, while that of H_2O source was 23°C.

ii) N_2 flow rate through $SnCl_4$ was 550 cc/min, and through H_2O was 1250 cc/min, for samples at Sl.Nos.1-36. In case of samples at Sl.Nos. 37-40 (marked with astrix), N_2 flow through $SnCl_4$ and H_2O was doubled compared with other samples.

probably be achieved by increasing source temperature to enable higher concentration of reacting species to reach the substrate. Table 2.1 also indicates that though Sb doping helped in reducing electrical resistivity of SnO_2 films, the film properties showed no particular trend with N_2 flow rate through $SbCl_3$ source. This indicated that the amount of Sb incorporated in the film was not dependent on the amount transported by carrier gas, but probably was about the same for all the films deposited at about 300°C. Another probability was that the deposits on the furnace tube might have acted as source for dopant, since the films deposited on two samples, CNCT25 and CST6 (cf. Table 2.1), with no N_2 flowing through $SbCl_3$ resulted in about the same sheet resistance as obtained in case of Sb doped films. Very high flow rate of N_2 through $SbCl_3$ (> 150 cc/min) resulted in films with considerably reduced transmittance. Separate sets of furnace tube, attachments, boat and masks, etc. were therefore used during deposition of undoped and Sb doped films, to avoid unintentional doping of undoped films. Samples CNTO, CNT1, CNT2, CNT8 and a few heterojunctions were prepared by avoiding unintentional doping. The deposition rates of Sb doped films were about the same as those of undoped films, in the range of 10-30 Å/min (cf. Table 2.1). These deposition rates were smaller than usual growth rates observed in hydrolytic processes employed for deposition of SnO_2 films for

unsophisticated commercial applications. However, these deposition rates are comparable with growth rates obtained in case of sputtering and may be adequate for optoelectronic applications requiring highly transparent and conducting films of about 2000 Å. The deposition temperature of 300°C employed in sample fabrication is lower compared with those generally used in hydrolytic processes and may be an added advantage in fabrication of optoelectronic devices.

Electrical Properties :

The electrical properties of undoped and Sb-doped SnO_2 films deposited by chemical vapor deposition are shown in Table 2.1. All the films showed n-type conductivity by hot and cold probe technique. Undoped SnO_2 films deposited for about 50 min. on polished n-type silicon substrates resulted in sheet resistance of 215-270 Ohm/sq. These films had estimated thickness of about 1000 Å. Resistivity of a 3000 Å thick undoped SnO_2 film, sample CNT8, deposited for 120 min., was found to be 2.9×10^{-3} Ohm.cm. Most of Sb-doped SnO_2 films had sheet resistance in the range of 100-300 Ohm/sq. The lowest value of sheet resistance obtained for such films was 44 Ohm/sq. (cf. Table 2.1). The large variation in sheet resistance was due to a large variation in film thickness deposited under apparently similar conditions. This was probably due to uncontrollable variation in substrate temperature during different runs. The temperature of the furnace varied rapidly in the

region where deposition was carried out. The position of boat in the furnace tube, and the position of substrates on the boat, could not be controlled very precisely, and the substrate temperature variation could have been within $\pm$ 30°C. A properly designed reaction chamber would overcome this problem. The resistivity of most of the Sb doped SnO_2 films were, however, in a narrow range of $(1.0-2.0)\times10^{-3}$ Ohm-cm. Undoped SnO_2 films also showed a narrow resistivity range. This implies that, though the film thickness was not well controlled because of above mentioned reasons, the film resistivity was well controlled. The lowest value of resistivity in case of Sb doped SnO_2 film was 8.6×10^{-4} Ohm-cm for a 1430 Å thick film having a sheet resistance of 60 Ohm/sq. A few samples gave higher values of resistivity in the range of $(2.0-4.0)\times10^{-3}$ Ohm-cm, which incidentally had longer deposition time and lower flow of N_2 through $SbCl_3$. A trend worth mentioning, though not very significant, was that deposition for longer than 60 min duration resulted in slightly higher film resistivity compared to that deposited for 60 min. during the same run. This can be seen from Table 2.1 which gives two such sets of samples namely CNOT 26-29 and CNOT 35-37. This might be related to the effect of prolonged heat treatment of the film in oxidizing ambient during deposition. Comparison of resistivity data of undoped and Sb doped SnO_2 films from Tables 2.1 reveals that though Sb doping reduced the resistivity

of the film, the difference was not large . Probably a substrate temperature of about 300°C does not incorporate sufficient Sb ions in the film to bring down the resistivity appreciably. Still, the resistivities obtained for both undoped and Sb doped SnO_2 films, are very encouraging and amongst lowest reported in literature for films prepared by hydrolysis [17,36,39,41,46,47,60,72-83].

Optical Properties :

The average transmission for undoped SnO_2 films deposited during initial trial runs was found to be in the range of 85--90% for visible light. After deposition parameters were adjusted, Sb doped SnO_2 films were deposited on polished fused silica substrates. All the films on fused silica substrates, samples CST 1-8, showed very high transmittance. Optical transmission of two such samples, CST 1 and CST 3, measured as a function of incident wavelength using Cary 17 D spectrophotometer, are shown in Figures 2.3(a) and 2.3(b) respectively. The films showed absorption in ultraviolet region and exhibited more than 90% transmission in visible and near infrared region. Such a high transmission for Sb doped SnO_3 films prepared by hydrolysis and having sheet resistance value of less than 200 Ohm/sq has been reported only by a few investigators [41,46,78,80]. The optical bandgap has been determined from absorption characteristics of these films in ultraviolet

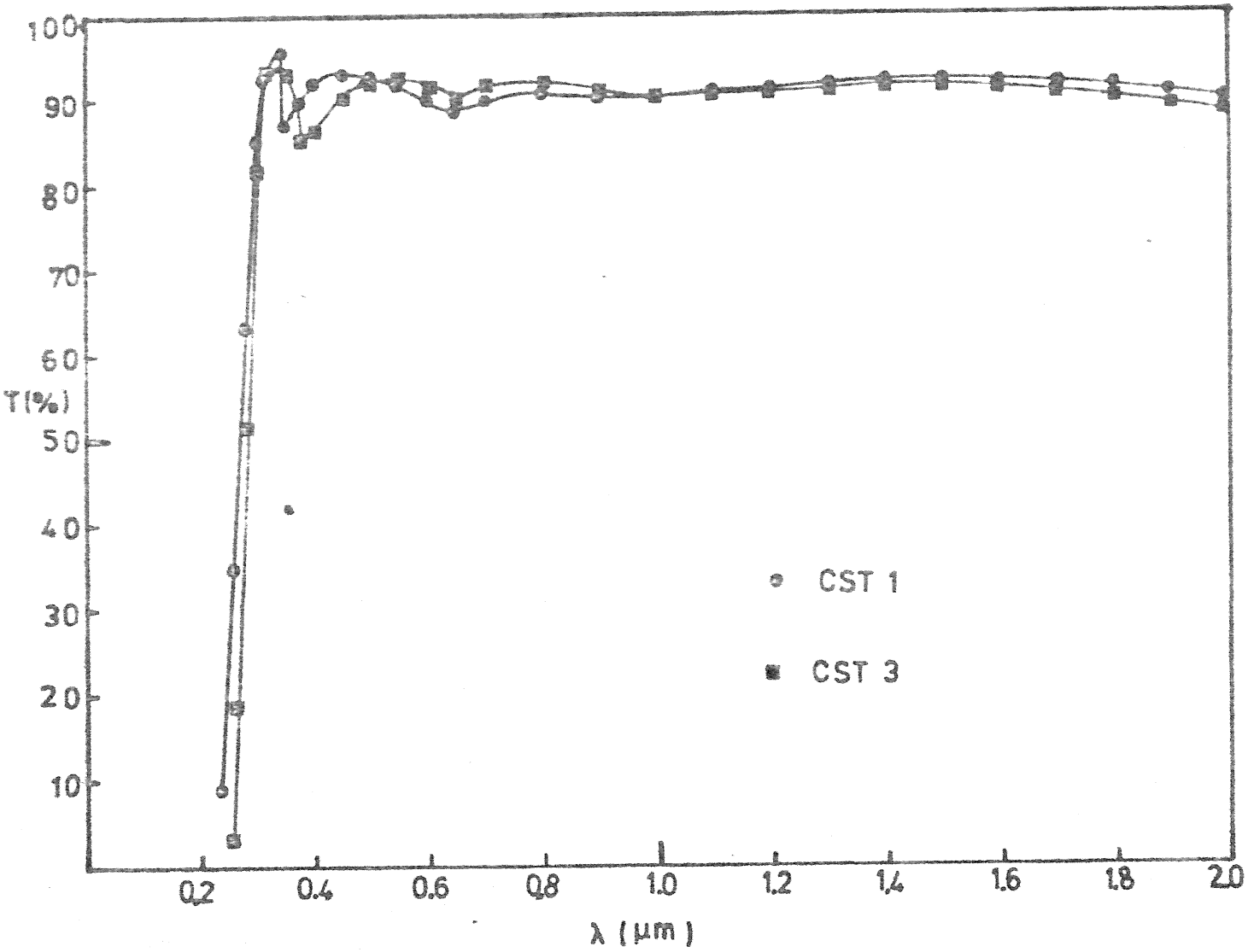


Figure 2.3 Measured optical transmission as a function of incident radiation wavelength of typical Sb doped SnO_2 films deposited by C.V.D on polished fused SiO_2 substrate. (a) Sample CST1 and (b) Sample CST 3

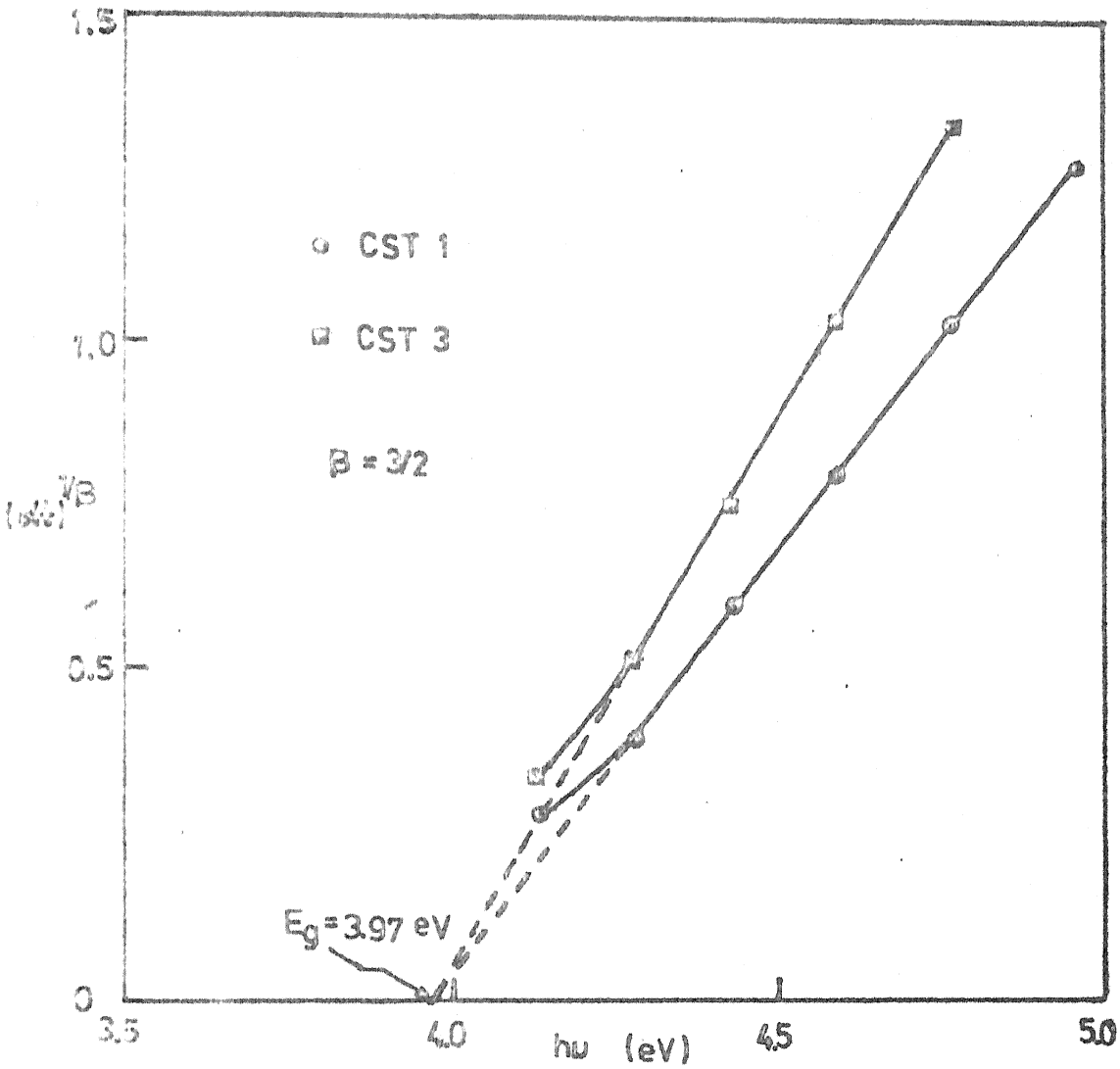


Figure 2.4 $(\alpha t)^{1/B}$ vs hω plots for samples (a) CST1 and (b) CST 3 calculated from optical transmission vs wavelength data

region as discussed in Section 2.3.3. Figure 2.4 shows the plots of $(\alpha t)^{1/B}$ vs $h\nu$, for samples CST 1 and CST 3, which show straight lines for both cases with B = 3/2 with the intercept at α = o giving the optical bandgap. Both the samples gave an optical bandgap of 3.97 eV which matches well with the reported value of 4.10 eV obtained for Sb doped SnO_2 films prepared by spray hydrolysis [75]. Undoped SnO_2 films prepared by spray hydrolysis have been reported with bandgap of 3.70 eV [17] and antimony doping has been found to increase the bandgap of SnO_2 films [47]. Though various investigators have reported direct optical bandgap of 3.70-4.30 eV for SnO_2 films prepared by different techniques [2,17,75], energy band investigations [58,59] show the possibility of both direct and indirect optical transitions. The value of B = 3/2 obtained under present investigation indicates the most probable absorption by indirect transition.

Structural Characterization :

Tables 2.2 - 2.5 summarise X-ray diffraction data for undoped sample CNT 2 and Sb doped samples CNOT15, CNOT20, and CNOT21, respectively. X-ray data unfortunately cannot be used for very accurate identification of various phases in thin films. Since these oxides are nonstoichiometric and contain dopant which is likely to be incorporated as a substitutional impurity, very good matching of d values from the standard data cannot be expected. Relative intensities also cannot be

2.2 : X-ray diffraction data for undoped SnO_2 sample CNT 2 (Bright interference colours, sample annealed in N_2 at 300°C for 60 min)

Observed Peaks				Identified phase using standard X-ray data for powder sample[71]			
2θ (°)	I (AU)	I/I_1	d (Å)	Material	d (Å)	I/I_1 std.	(hkl)
28.36	40	16	3.147	Si	3.138	100	(111)
31.55	155	63	2.836	SnO(O)	2.86	20	(020)
32.40	45	18	2.763	SnO(O)	2.78	40	(004)
34.00	100	41	2.636	SnO_2	2.644	81	(101)
36.04	246	100	2.492	SnO(O)	2.50	30	(200)
47.31	55	22	1.921	Si	1.920	60	(220)
51.81	85	35	1.765	SnO_2	1.765	63	(211)
56.39	105	43	1.632	Si	1.638	35	(311)
62.66	70	29	1.483	SnO_2	1.498	13	(310)
66.06	45	18	1.414	SnO_2	1.415	15	(301)
67.74	60	24	1.383	SnO(O)	1.393	20	(008),(042)
68.88	29	12	1.363	Si	1.357	8	(400)

Table 2.3 : X-ray diffraction data for Sb doped SnO_2 sample CNOT 15 (Bright interference colours)

Sl. No.	Observed Peaks				Identified phase using standard X-ray data for powder sample [71]			
	2θ (°)	I (AU	I/I_1	d (Å)	Material	d (Å)	I/I_1 std.	(hkl)
1.	28.28	60	1.0	3.155	Si	3.138	100	(111)
2.	31.50	157	2.6	2.841	SnO(O)	2.86	20	(020)
3.	34.16	84	1.4	2.625	SnO_2	2.644	81	(101)
4.	36.00	210	3.4	2.495	SnO(O)	2.50	30	(200)
5.	47.26	46	0.8	1.922	Si	1.920	60	(220)
6.	47.66	172	2.8	1.908	SnO(O)	1.888	20	(220)
7.	54.56	380	6.2	1.682	SnO(O)	1.681	30	(223)
8.	55.42	131	2.1	1.658	SnO(O)	1.662	20	(116)
9.	56.32	900	14.6	1.634	Si	1.638	35	(311)
10.	57.28	94	1.5	1.607	SnO(O)	1.610	20	(133)
11.	61.70	6170	100	1.503	SnO_2	1.498	13	(310)
12.	65.83	2134	34.6	1.419	SnO_2	1.415	15	(301)
13.	66.40	154	2.5	1.408	SnO(O)	1.393	20	(008),(042)
14.	69.00	Very High	>100	1.361	Si	1.357	8	(400)

Table 2.4 : X-ray diffraction data for Sb doped SnO_2 sample CNOT 20 (Hazy film)

Sl. No.	Observed Peaks				Identified phase using standard X-ray data for powder sample [71]			
	2θ (o)	I (AU)	I/I_1	d (Å)	Material	d (Å)	I/I_1 std.	(hkl)
1.	25.42	53	23	3.505	SnO(O) Sb_2O_4	3.58 3.452	30 35	(111) -
2.	28.26	204	90	3.157	Si	3.138	100	(111)
3.	31.48	164	72	2.842	SnO(O)	2.86	20	(020)
4.	32.36	52	23	2.766	SnO(O)	2.78	40	(004)
5.	34.16	106	47	2.626	SnO_2	2.644	81	(101)
6.	36.00	228	100	2.495	SnO(O)	2.50	30	(200)
7.	47.29	66	29	1.922	Si	1.920	60	(220)
8.	50.50	23	10	1.807	Sb_2O_4	1.801	8	-
9.	51.78	63	28	1.766	SnO_2	1.765	63	(211)
10.	56.38	113	50	1.632	Si	1.638	35	(311)
11.	62.66	73	32	1.483	Sb_2O_5	1.488	10	(444)
12.	66.06	30	13	1.414	SnO_2	1.415	15	(301)
13.	67.74	66	29	1.383	SnO(O)	1.393	20	(008),(042
14.	69.00	51	21	1.361	Si	1.357	8	(400)

Table 2.5 : X-ray diffraction data for Sb doped SnO_2 sample CNOT 21 (Bright interference colours)

Sl. No.	Observed Peaks				Identified phase using standard X-ray data for powder sample [71]			
	2θ (o)	I (AU)	I/I_1	d (Å)	Material	d (Å)	I/I_1 std.	(hkl)
1.	31.40	148	42	2.849	SnO(O)	2.86	20	(020)
2.	32.30	40	11	2.771	SnO(O)	2.78	40	(040)
3.	34.12	95	27	2.628	SnO_2	2.644	81	(101)
4.	35.92	215	61	2.500	SnO(O)	2.50	30	(200)
5.	38.02	35	10	2.367	Sb_2O_5	2.365	4	(331)
6.	47.23	54	15	1.924	Si	1.920	60	(220)
7.	51.72	38	11	1.767	SnO_2	1.765	63	(211)
8.	56.31	95	27	1.634	Si	1.638	35	(311)
9.	61.61	352	100	1.505	SnO_2	1.498	13	(310)
10.	62.60	58	16	1.484	Sb_2O_5	1.488	10	(444)
11.	65.83	225	64	1.419	SnO_2	1.415	15	(301)
12.	67.71	45	13	1.384	SnO(O)	1.393	20	((008),(042
13.	69.08	Very High	>100	1.360	Si	1.357	8	(400)

used as a guideline in case of thin films with strong possibility of preferred orientation. At times more than one phase show d values close to those obtained from X-ray diffraction and the investigator has to use his own judgement regarding most probable phase. We have considered the phases already identified through other peaks in the same or similar samples as the most probable phase. The phases volatile at deposition temperatures have been ruled out. Upon inspecting Tables 2.2 - 2.5 together we observe that some peaks in all the films are due to diffraction from silicon substrate. Other peaks are mostly from SnO_2 and SnO (orthorhombic) phases. SnO can crystallize in either tetragonal or orthorhombic phase depending on deposition conditions. The deposition conditions in present investigation seem to have favoured SnO (orthorhombic) phase. Sb doped films show some weak peaks which might be from Sb and its oxides like Sb_2O_5, Sb_2O_4 etc. Sb and its oxides at times have very close d values and the differentiation becomes difficult. We have considered the presence of Sb in elemental form under oxidizing conditions as a remote possibility and have identified the peaks due to reflections from Sb_2O_5 and Sb_2O_4 phase.

Identification of peaks was relatively easy in case of undoped film, sample CNT2 whose X-ray diffraction data are presented in Table 2.2. Silicon reflections have been identified from (111), (220), (311) and (400) planes. SnO_2 reflections have been identified from planes (101), (211), (310)

and (301) planes, while SnO (O) reflections have been identified from (020), (004), (200) and (008/042) planes. In this sample the reflections from SnO (O) (200) and (020) planes are very strong followed by reflections from Si (311) plane and SnO_2 (101), (211), and (310) planes. Remaining reflections were relatively weaker.Sb-doped films, samples CNOT 15, CNOT 20 and CNOT 21 also show the above mentioned peaks. Sample CNOT 15 showed strongest reflection from Si (400) plane followed by those from SnO_2 (310), (301) planes and Si (311) plane. All other reflections were very weak (cf Table 2.3). Some of the weak reflections are SnO (O) (220), (223), (116), and (133) planes which have not been detected in other films. In case of sample CNOT 20 (cf. Table 2.4), strongest reflections are from SnO(O) (200), Si (111), SnO (O) (020), Si (311) and SnO_2 (101) planes. This sample also shows moderate intensity of reflection from Sb_2O_5 (444) plane. Another feature of this sample is a moderate intensity peak at 2θ value of 25.42° which has not been observed in other samples. This could be due to SnO (O) (111) plane or might be arising from some oxide of Sb like Sb_2O_4, though they donot match well with the d value obtained. Sb_2O_4 is likely to have resulted in a relatively week reflection at 2θ value of 50.50° also. Sample CNOT 21 (cf. Table 2.5) showed strongest reflection from Si (400) plane followed by that from SnO_2 (310), (301), planes and SnO(O) (200) and (020) planes. This sample also showed weak reflections from Sb_2O_5 (444) and (331) planes

in addition to some from SnO_2, SnO(O) and Si planes as in case of other samples.

It is interesting to note that in samples CNOT 15 and CNOT CNOT 21 where SnO_2 peaks were strongest (leaving Si peaks due to substrate), the films showed very good reflectivity and bright interference colours. Sample CNOT 20 on the other hand showed strong reflections from SnO(O) planes, and some moderate and weak reflections from oxides of antimony. This sample, incidentally, showed some haze, probably due to antimony oxides and/or SnO(O) phases. Sample CNT 2 was given a heat treatment in N_2 at 300°C for 60 min, which might have resulted in excess SnO phases giving rise to intense reflections.

In summary, the films deposited by chemical vapor deposition showed strong preferred orientation for SnO_2 as well as SnO(O) phases. Apart from silicon reflections from (111),(220), (311) and (400) planes, the X-ray data revealed SnO_2 reflections from (101), (211), (310), and (301) planes and SnO(O) reflections from (020), (004), (200) and (008/042) planes. Weaker reflections from Sb_2O_5 (331) and (444) planes were also observed in Sb doped samples. Preferred orientation has been found in case of SnO_2 films by other investigators also [4,44, 46]. Low temperature deposition probably resulted in incomplete oxidation of Sn resulting in SnO phase. Higher deposition temperature may result in lower concentration of SnO phase in the film.

The electron diffraction patterns of SnO_2 films deposited on silicon substrates showed spotty rings indicating polycrystalline nature of film. The electromicrographs also showed polycrystalline films with uniform grains all over the film. These micrographs have been used to determine the grain size in these films. Table 2.6 summarises the grain size data for these films. It shows that the grain size for undoped films was in the range of 900-1450 Å. It compares well with the grain size value of 1000 Å obtained on chemical vapor deposited undoped SnO_2 film at 380°C by Aboaf et al [36], who also found that the grain size increased with increase in deposition temperature. The grain size of Sb doped films (cf. Table 2.6) were smaller compared to undoped films and were in the range of 540-720 Å. Shanthi et al [46] observed that the grain size of spray deposited Sb doped SnO_2 films, formed at 540°C, increased from 250 Å till 600 Å as Sb doping increased, and then saturated. The film resistivity was also found to decrease from $2x10^{-2}$ Ohm cm to $2x10^{-3}$ Ohm cm with Sb doping. We have found that in case of chemical vapor deposited films formed at 300°C, Sb doping level neither changed the resistivity nor the grain size appreciably. Higher grain size obtained at lower deposition temperature under present investigation compared to those reported [46] show superiority of chemical vapor deposition over spray hydrolysis. With the rise in substrate temperature, the grain size of chemical vapor deposited samples is

Table 2.6 : Grain size data of chemical vvapor deposited SnO_2 films

Sl. No.	Sample No.	N_2 flow through $SbCl_3$ (cc/min)	Thickness (Å)	R_{sh} Ohm/sq	Resistivity (Ohm-cm)	Grain size (Å)
1.	CNOT 8	-	-	-	-	900
2.	CNOT 25	-	-	180	-	1450
3.	CNOT 30	-	960	610	5.9×10^{-3}	900
4.	CNOT 31	6	580	310	1.8×10^{-3}	720
5.	CNOT 26	11	980	265	2.6×10^{-3}	540
6.	CNOT 32	11	350	430	1.5×10^{-3}	360
7.	CNOT 17	18	-	185	-	630
8.	CNOT 14	28	830	190	1.6×10^{-3}	720
9.	CNOT 16	28	620	270	1.7×10^{-3}	720
10.	CNOT 34	28	860	175	1.5×10^{-3}	540
11.	CST 3	28	-	175	-	610
12.	CNOT 11	40	535	210	1.1×10^{-3}	630
13.	CNOT 13	40	720	185	1.3×10^{-3}	540

expected to rise and hence, Hall mobility should also be more in case of these samples compared to those deposited by spray hydrolysis.

Comparison of present investigation with results reported in Literature :

Table 2.7 summarises important properties of SnO_2 films prepared by hydrolysis process as reported by various investigators and those obtained during present investigation. Most of the investigators have used deposition temperature of 400--600°C, though some have used even upto 700°C. We have used a low deposition temperature of 300°C which may offer advantage for optoelectronic device fabrication. The deposit films showed presence of SnO phase also probably due to incomplete oxidation of Sn at such a low temperature. SnO phase has been reported by other investigators also but some conflicting results are also reported [2]. Presence of SnO phase probably depends on deposition conditions. Our films showed preferred orientation as has been reported by other investigators [4,44,46]. An interesting observation is that we have found grain size of 900-1450 Å for undoped film which compares well with the value shown for similar film in Table 2.7 [36]. The grain size for Sb doped film is lower compared to undoped film but compared well with spray deposited Sb doped films formed at 540°C [46]. The resistivity of undoped SnO_2 film deposited by hydrolysis process has been reported to be is th

Table 2.7 : Important properties of SnO_2 film deposited by spray hydrolysis and chemical vapor deposition as reported in literature

Sl.No.	Technique [Reference]	Dopant (m/o)	Dep. Temp. (°C)	t (Å)	T (%)	λ (μm)	R_{sh} (Ohm/sq)	ρ (Ohm cm)	μ_H ($cm^2V^{-1}sec^{-1}$)	Remarks
1	2	3	4	5	6	7	8	9	10	11
1.	Spray [17]	-	450-500	6000	80-90	Av.	-	5×10^{-3}	-	E_g = 3.7 eV
2.	CVD [36]	-	400 600	2000	-	-	-	7×10^{-3} 1.1×10^{-2}	-	Grain size 1000Å at 380°C and increased with deposition temp.
3.	CVD [39]	-	400	3600-11000	80-95	0.40-0.65	-	1×10^{-2}	-	-
4.	CVD [41]	Sb (0.6-2.7)	400-550	1500-3600	85-91	Av.	50-150	1.5×10^{-3} 3.2×10^{-3}	23	n=1.89, pyrolysis process
5.	Spray [46]	- Sb (1.4)	540 540	3500 3500	84 90-95	0.70 0.55	- -	2×10^{-2} 2×10^{-3}	7 15	Grain size increased from 250 Å to 600 Å with doping level and then saturated

contd ...

1	2	3	4	5	6	7	8	9	10	11
6.	Spray [47]	-	540	3500	80	0.60	> 500	2×10^{-2}	7	
		Sb(3)	540	3500	60	0.60	60	2.1×10^{-3}	15	
		Sb(10)	540	3500	35	0.60	300	1×10^{-2}	1	
		F (20)	540	6000	80	0.50-0.70	18	1.1×10^{-3}	23	
		F (50)	540	6000	80	0.50-0.70	13	7.2×10^{-4}	23	
		F (65-80)	540	6000	80	0.50-0.70	8	4.8×10^{-4}	23	
7.	Spray [60]	F	-	-	80	0.50-0.70	8.6	-	46	
8.	Spray [72]	-	-	1100	-	-	-	2.3×10^{-3}	29	
9.	Spray [73]	-	400	3500	-	-	-	6.0×10^{-3}	-	Post deposition annealing at 300°C reduced resistivity
10.	Spray [74]	Sb(0.4)	650	-	-	-	-	9×10^{-4}	35	
		Sb(1.0)	650	-	-	-	-	7×10^{-4}	30	
		Sb(7.0)	650	-	-	-	-	1.5×10^{-3}	8	
		Sb(11.0)	650	-	-	-	-	8×10^{-3}	3	

contd ...

1	2	3	4	5	6	7	8	9	10	11
11.	Spray [75]	Sb(1.5)	700	-	-	-	-	1.0×10^{-3}	20	E_g = 4.1 eV
12.	Spray [76]	Sb(1.0)	550	-	-	-	-	3.3×10^{-3}		
13.	Spray [77]	Sb(0.2)	600	-	-	-	-	2.1×10^{-3}	-	-
		Sb(0.6)	600	-	-	-	-	9.7×10^{-4}		
		Sb(1.7)	600	-	-	-	-	1.23×10^{-3}	-	-
		Sb(5.4)	600	-	-	-	-	1.62×10^{-3}	-	-
		Sb(13.0)	600	-	-	-	-	1.32×10^{-2}	-	-
14.	Spray [78]	-	500	-	60	Av	100	-	-	-
		-	500	-	70	Av	200	-	-	-
		-	500	-	80	Av	800	-	-	-
		Sb(0.4)	500	-	65	Av	20	-	-	-
		Sb(0.4)	500	-	82	Av	50	-	-	-
		Sb(0.4)	500	-	88	Av	80	-	-	-
		Sb(0.4)	500	-	90	Av	200	-	-	-
15.	Spray [79]	-	500	-	80-90	0.50-2.0	85	5×10^{-3}	13	
		F(1.3)	500	-	85	0.50-2.0	10.6	5.6×10^{-4}	10.6	

contd ...

1	2	3	4	5	6	7	8	9	10	11
16.	Spray [80]	Sb(1.5)	600	> 4000	90	0.60	-	9.5×10^{-4}	9.6	SiO_2 substrate
					90	0.60	-	8.6×10^{-4}	9.6	Borosilicate substrate
					75	0.60	-	1.8×10^{-3}	2.0-9.5	Alkali glass substrate
17.	Spray [81]	F	-	-	80-90	0.50-1.2μm	-	-	20	
18.	CVD [82]	Sb	450	-	-	-	50	-	-	
19.	CVD [83]	-	-	-	90-95	Av.		5×10^{-3}	10	n=1.75 to 2.20 varying inversely with thickness, Pyrolysis process
20.	CVD present investigations	-	300	900-1400	85-90	Av.	460-700	5.1×10^{-3} -7.3×10^{-3}	-	H_2O source at 93°C
		-	300	-		-	215-270	-	-	H_2O source at 23°C Grain size 900-1450 Å
			300	3000	-	-	98	2.9×10^{-3}	-	Minimum resistivity
		Sb	300	300-2000	90-95	0.40-1.80	100-300	$1.0-2.0\times10^{-3}$	-	H_2O source at 23°C Grain size 540-720Å E_g = 3.97 eV
		Sb	300	1430	-	-	60	8.6×10^{-4}	-	Minimum resistivity

in the range of $5x10^{-3}$ to $2x10^{-2}$ Ohm-cm depending on deposition conditions (cf Table 2.7). Our resistivity value of $2.9x10^{-3}$ Ohm-cm for undoped SnO_2 film seems to be the lowest value reported for such films. The resistivity of Sb doped film has been reported to depend on Sb doping level [46,47,74,77]. Different investigators have found minimum resistivity for Sb doping in the range of 1.5-3.0 m/o (cf. Table 2.7). The resistivity of Sb doped film has been generally reported to be in the range of $7x10^{-4}$ - $3x10^{-3}$ Ohm-cm for optimum doping. We have also obtained similar resistivity for Sb doped SnO_2 films, though the deposition temperature is lower than that used by other investigators. Another feature which is clear from Table 2.7 is that optical transmission in the range of 90-95% in visible and near infrared region for films with sheet resistance less than 200 Ohm/sq, has been obtained by only few investigators [46,78,80,83]. The optical quality of our films also seems to be amongst the best reported for such films. The value of optical bandgap obtained as 3.97 eV during present investigation also matches well with that reported for similar film [75]. In summary we can say that though we have deposited undoped and Sb doped films at temperatures of about 300°C which are considerably lower compared to those used by other investigators, the opto-electronic properties of these films are amongst the best reported in literature for films deposited by similar chemical processes.

2.4.2 Properties of E-beam deposited Sn doped In_2O_3 films

The main emphasis was on adjusting deposition parameters so as to get good quality transparent conducting film. The effect of various deposition parameters on the electrical properties of Sn doped In_2O_3 films are summarized in Table 2.8.

Initial deposition runs were carried out in residual air atmosphere at substrate temperature of about 300°C. The pressure during deposition was in the range of $1\text{-}2\times10^{-5}$ torr. The films deposited on silicon and fused silica substrates were soft, less reflecting, opaque and with metallic lusture. Post deposition annealing in oxygen at about 400°C resulted in transparent film on SiO_2 substrate, sample ESI-1, and improved reflectivity and interference colours on films on silicon substrates. The hardness of the films also improved with oxidation. The sheet resistance of oxidized films was in the range of 30-60 Ohm/sq. Annealing in oxygen at a temperature of 450°C for 60 min, following initial post deposition annealing at 400°C for 120 min, was found to increase the sheet resistance of sample EP01-3 from 30 Ohm/sq to 39 Ohm/sq, indicating that higher temperature or prolonged heat treatment in oxygen may adversely affect film resistivity. The film deposited at room temperature resulted in considerably high sheet resistance of 375 Ohm/sq even after the subsequent oxidation. This indicated that deposition at elevated substrate temperatures favoured high conductivity. The opacity, softness, and metallic nature of

Table 2.8 : Effect of deposition parameters on properties of E-beam deposited Sn doped In_2O_3 films

Sl. No.	Sample No.	Deposition				Post-deposition annealing					Remarks
		Ambient	O_2 partial pressure ($\times 10^{-6}$ Torr)	Time (min)	R_{sh} (Ohm/sq	Run No.	Ambient	Temp. (°C)	Time (min)	R_{sh} (Ohm/sq)	Remarks
1	2	3	4	5	6	7	8	9	10	11	12
1.	EPI-1	Res Air	-	45	-	a	O_2	400	60	45	As deposited: metallic soft, non reflecting. Annealed: refl., Hard, Blue,
2.	ENI-1	Res.Air	-	45	-	a	O_2	400	120	51	Same as in EPI-1
3.	ESI-1	Res.Air	-	45	-	a	O_2	400	60	62	As dep: opaque Annealed: transp.
4.	EPCI-2	Res.Air	-	45	-	a	O_2	400	60	55	Refl.improved upon annealing
5.	EPCI-3	Res.Air	-	70	-	a	O_2	400	60		As dep: thick, soft, non refl.,
						b	O_2	400	60	30	Annealing(a+b):Reft. slightly soft.
						c	O_2	450	60	39	(c) : no change
6.	EPCI-4	Res.Air	-	75	-	a	O_2	400	60	375	RT deposition
7.	ESI-2	O_2	5	45	62	-	-	-	-	-	Very transparent
8.	ESI-3	O_2	5	60	27	a	O_2 (7×10^{-3} Torr)	400	30	25	No change on annealing a and b
						b	H_2 (7×10^{-3} Torr)	400	30	25	

contd ....

1	2	3	4	5	6	7	8	9	10	11	12
9.	EPI-2	O_2	5	45	60	a	O_2	400	30	66	
10.	ENI-3	O_2	5	60	22	a	H_2+N_2 (1:4)	500	60	21	Refl.improved with annealing
11.	EPI-3	O_2	5	60	21	-	-	-	-	-	Moderately Refl.film
12.	ENI-6	O_2	5	60	-	a	Res Air (7×10^{-7} torr)	300	45	54	Very reflecting film with no effect of annealing
						b	O_2 (7×10^{-3} torr)	400	30	51	
						c	H_2 (7×10^{-3} torr)	400	30	51	
13.	ENI-7	O_2	5	60	-	a	Res Air (7×10^{-7} torr)	300	45	62	Very refl. film with no affect of annealing
						b	N_2	450°C	30	-	
						c	H_2+N_2 (1:4)	450°C	30	55	

contd ...

1	2	3	4	5	6	7	8 8	9	10	11	12 12
14.	ENI-8	O_2	5	60	-	a	Res Air (7×10^{-7} torr)	300	45	57	no effect of annealing on film refl.
						b	H_2 (7×10^{-3} torr)	400	30	54	
						c	N_2	550	30	-	
						d	H_2+N_2 (1:4)	450	30	75	
15.	ENI-10	O_2	8	60	33	-	-	-	-	-	refl. moderate
16.	ENI-13	O_2	10	60	-	a	N_2	650	30	-	As dep.film very refl.with no change due to annealing
						b	H_2+N_2 (1:4)	500	30	140	
17.	ENI-14	O_2	10	60	-	a	N_2	650	30	291	As dep.film very refl.,no change due to annealing
						b	H_2+N_2 (1:4)	500	60	153	
18.	ESI-7	O_2	10	60	-	a	Ar (7×10^{-3}torr)	400	30	-	As dep.film very transparent. Annealing made no diff.
19.	ENI-15	O_2	10	60	96	a	Ar (7×10^{-3}torr)	400	30	93	As dep.film very refl. Annealing made no diff.
						b	H_2+N_2 (1:4)	450	30	120	

as deposited films indicated that during e-beam evaporation, Sn doped In_2O_3 got reduced resulting in probably unoxidized In atoms in the film. Subsequent heat treatment in oxidizing ambient resulted in transparent conducting films due to oxidation of these In atoms.

Subsequent depositions were carried out in oxygen partial pressure. Deposition of film on SiO_2 substrate, sample ESI-2, in oxygen partial pressure, resulted in very transparent film eliminating the need for post deposition oxidation. Film deposited on SiO_2 substrates with oxygen partial pressure of $5x10^{-6}$ torr resulted in sheet resistance of 62 Ohm/sq for a film deposited for 45 min (sample ESI-2) and sheet resistance of 27 Ohm/sq for a film deposited for 60 min (sample ESI-3). Both these films were highly transparent. Post deposition heat treatments of sample ESI-3 in oxygen and hydrogen partial pressures at a temperature of 400°C for 30 min each did not affect the sheet resistance of as deposited film appreciably (cf Table 2.8). Post deposition heat treatments in oxygen, mixture of hydrogen and nitrogen, oxygen partial pressure and hydrogen partial pressure, did not seem to affect sheet resistance of these films, appreciably, as is evident from the results of various heat treatments summarised in Table 2.8. However, the reflectance of the films in general was found to be improved by heat treatments. The sheet resistance data indicated that the films deposited in oxygen partial pressure

were quite stable and heat treatments in oxidizing or reducing ambient did not effect the film properties appreciably. In case of samples deposited with oxygen partial pressure of 5×10^{-6} torr during deposition, the sheet resistance values were found to be in the range of 20-25 Ohm/sq for most of the samples deposited for 60 min, and in the range of 60-65 Ohm/sq for samples deposited for 45 min. Samples ENI 6-8 were deposited for 60 min under above conditions and then given a heat treatment in residual air at a pressure of 7×10^{-7} torr inside vacuum system. The sheet resistance for these samples after heat treatment in vacuum showed values in the range of 50-60 Ohm/sq, which are higher compared to those obtained in as deposited films. This shows that vacuum annealing might have adversely affected the film resistivity. Subsequent heat treatment in oxidizing or reducing atmosphere showed slight decrease in film resistivity of samples ENI-6 and ENI-7. In case of sample ENI-8, the post deposition heat treatment in hydrogen reduced the sheet resistance slightly but subsequent heat treatments in N_2 and N_2+H_2 increased sheet resistance. These results show some ambiguity about the effect of heat treatment in oxidizing, reducing as inert atmosphere on films deposited in oxygen partial pressure followed by heat treatment in vacuum.

Sample ENI-10 which was deposited at oxygen partial pressure of 8×10^{-6} torr showed a sheet resistance of 33 Ohm/sq. Depositions at higher partial pressure ofoxygen, such as 1×10^{-5} torr, resulted in films with considerably higher sheet resistance (cf. Table 2.8). This indicated that the sheet resistance of films increased with increase in oxygen partial pressure. Oxygen partial pressure of 5×10^{-6} torr has given best films which didnot require any further heat treatment.

Samples ENI-13 and ENI-14 were subjected to post deposition heat treatment in N_2 followed by that in N_2+H_2 (4:1). The results obtained after final heat treatment in both cases show about same sheet resistance. However, the value of sheet resistance in case of sample ENI-14 measured after heat treatment in N_2 shows relatively higher value. This indicates that probably heat treatment in reducing atmosphere, in case of samples deposited with high oxygen partial pressure, improved the conductivity of the films. The sheet resistance of sample ENI-15 annealed in Ar partial pressure after deposition,however, showed slight increase in sheet resistivity due to subsequent heat treatment in reducing atmosphere.

Electron-beam deposited films had thickness of about 2000 Å, and hence the best films had resistivity of less than 1×10^{-3} Ohm-cm.

2.5 CONCLUSION

Chemical vapor deposition at substrate temperatures of about 300°C has been employed to deposit very good quality undoped and Sb doped SnO_2 films. The sheet resistance of undoped SnO_2 films in general were in the range of 215-270 Ohm/sq, while the minimum value of sheet resistance of a 3000 Å thick film was 98 Ohm/sq resulting in resistivity of about 3×10^{-3} Ohm-cm. The resistivity of Sb doped SnO_2 films on silicon and fused silica substrates were generally in the range of $(1-2) \times 10^{-3}$ Ohm-cm though the lowest value of resistivity obtained was 8.6×10^{-4} Ohm-cm for a 1430 Å thick film. All these films had thickness in the range of 500-2000 Å with most of the films in the range of 1000-1500 Å thickness. Deposition rates obtained were in the range of 10-30 Å/min for both types of films. Undoped films had a grain size of about 900-1450 Å while doped films had a grain size of about 540-720 Å. These films showed presence of SnO phase and same Sb_2O_5 phase in case of doped films. All the films showed preferred orientation. The optical transmission was found to be in the range of 90-95% in visible and near infrared region for Sb doped SnO_2 films. The optical bandgap of Sb doped SnO_2 film was found to be 3.97 eV. Thus the opto-electronic properties of these films are amongst the best reported in the literature, even though considerably lower substrate temperatures have been employed. The deposition rate, though lower compared to

did not show appreciable change in film resistivity and the films seem to be quite stable. Such a low value of sheet resistance in case of e-beam deposited Sn doped In_2O_3 films make them very suitable for optoelectronic devices. The resistivity of these films is estimated to be less than $1x10^{-3}$ Ohm-cm.

References

1. J.L. Vossen, Phys. Thin Films 9, 1 (1977).

2. K.L. Chopra, S. Major and D.K. Pandya, Thin Solid Films 102, 1 (1983).

3. G. Haacke, Ann. Rev. Mater. Sci. 7, 73 (1977).

4. J.C. Manifacier, Thin Solid Films 90, 297 (1982).

5. T. Feng, D.J. Eustace and A.K. Ghosh, Proc. 16th IEEE Photovoltaic Specialists Conf., XX (1982).

6. L. Holland and G. Siddal, Vacuum 3, 375 (1953).

7. H.K. Muller, Phys. Status Solidi 27, 723 (1968).

8. I. Hamberg, A. Hjorksberg and C.G. Granqvist, Proc. Soc. Photo-Opt. Instrum. Eng. 324, 32 (1982).

9. C.A. Pan and T.P. Ma, Appl. Phys. Lett. 37, 163 (1980).

10. T. Nishino and Y. Hamakawa, Jpn. J. Appl. Phys. 9, 1085 (1970).

11. H.U. Habermeier, Thin Solid Films 80, 157 (1981).

12. H.S. Randhawa, M.D. Mathews, and R.F. Bunshah, Thin Solid Films 83, 267 (1981).

13. D.E. Brodie, R. Singh, J.H. Morgan, J.D. Leslie, L.J.Moore and A.E. Dixon, Proc. 14th IEEE Photovoltaic Specialists Conf., 468 (1980).

14. P. Nath and R.F. Bunshah, Thin Solid Films 69, 63 (1980).

15. M. Mizuhashi, Thin Solid Films 76, 97 (1981).

16. M. Mizuhashi, J. Non-Crys. Solids 38-39, 329 (1980).

17. J.C. Manifacier, M. de Murcia, J.P. Fillard and E.Vicario, Thin Solid Films 41, 127 (1977).

18. E. Leja, A. Kolodziej, T. Pisarkiewicz and T. Stapinski, Thin Solid Films 76, 283 (1981).

19. N. Miyata, K. Miyake and S. Nao, Thin Solid Films 58, 385 (1979).

20. J.L. Vossen, J. Vac. Sci. Technol. 8, 751 (1971).

21. G.N. Advani, A.G. Jordan, and P. Kluge-Weiss, Mater. Sci. Eng . 4, 99 (1979).

22. A.G. Sabnis, J. Vac Sci. Technol. 15, 1565 (1978)

23. C.E. Wickersham and J. Greene, Phys.Status Solidi A47, 329 (1978).

24. J.C.C. Fan, F.J. Bachner, and G.H. Foley, Appl. Phys. Lett. 31, 773 (1977).

25. M. Buchanan, J.B. Webb and D.F. Williams, Appl.Phys. Lett. 37, 212 (1980).

26. D.B. Fraser and H.D. Cook, J. Electrochem. Soc. 119, 1368 (1972).

27. O. Caporaletti, Sol. Energy Mater. 7, 65 (1982).

28. G. Haacke, Appl. Phys. Lett. 28, 622 (1976).

29. J.C.C. Fan, Appl. Phys. Lett. 34, 515 (1979).

30. E. Giani and R. Kelly, J. Electrochem. Soc. 121, 394 (1974).

31. J.N. Avaritsiotis and R.P. Howson, Thin Solid Films 77, 351 (1981).

32. R.P. Howson, J.N. Avaritsiotis, M.I. Ridge, and C.A. Bishop, Thin Solid Films 58, 379 (1979).

33. J. Machet, J. Guille, P. Saulmier and S. Robert, Thin Solid Films 80, 149 (1981).

34. R.P. Howson, and M.I. Ridge, Thin Solid Films 77, 119 (1981).

35. R.N. Ghoshtagore, J. Electrochem. Soc. 125, 110 (1978).

36. J.A. Aboaf, V.C. Marcotte and N.J. Chou, J.Electrochem. Soc. 120, 701 (1973).

37. H. Kim and H.A. Laitinen, J. Am. Ceram. Soc. 58, 23 (1975).

38. O. Tabata, T. Tanaka, M. Waseda and K. Kinuhara, Surf. Sci. 86, 230 (1979).

39. T. Muranio, and M. Furukoshi, Thin Solid Films 48, 309 (1978).

40. R. Kalbskopf, Thin Solid Films 77, 65 (1981).

41. J. Kane, H.P. Schweizer and W. Kern, J.Electrochem. Soc. 123, 270 (1976).

42. L.A. Ryabova, and Ya. S. Savitskaya, Thin Solid Films, 2, 41 (1968).

43. L.A. Ryabova, V.S. Salun and I.A. Serbinov, Thin Solid Films 92, 327 (1982).

44. J.S. Maudes, and T.Rodriguez, Thin Solid Films 69, 183 (1980).

45. P. Grosse, F.J. Schmitte, G. Frank, and H. Kostlin, Thin Solid Films 90, 309 (1982).

46. E. Shanthi, V. Dutta, A. Banerjee, and K.L. Chopra, J. Appl. Phys. 51, 6243 (1980).

47. E. Shanthi, A. Banerjee, and K.L. Chopra, Thin Solid Films 88, 93 (1982).

48. J.C. Manifacier, L. Szepessy, J.F. Bresse and M. Perotin, Mater. Res. Bull. 14, 109 (1979).

49. R. Groth, Phys. Status Solidi 14, 69 (1966).

50. M.S. Tomar, and F.J. Garcia, Thin Solid Films 90, 419 (1982).

51. G. Haacke, H. Ando, and W.E. Mealmaker, J. Electrochem. Soc. 124, 1923 (1977).

52. S. Samson, and C.G. Fonstad, J. Appl. Phys. 44, 4618 (1973).

53. J.A. Marley and R.C. Dockerty, Phys. Rev. Sect.A 140, 304 (1965).

54. M. Nagaswa and S. Shionoya, Jap. J. Appl.Phys. 10, 727 (1971).

55. R.E. Aitchison, Acost. J. Appl. Sci. 5, 10 (1954).

56. Y.S. Hsu and S.K. Ghandi, J. Electrochem. Soc. 127, 1592 (1980).

57. Y.S. Hsu and S.K. Ghandi, J. Electrochem. Soc. 126, 1434 (1979).

58. F.J. Arlinghaus, J. Phys. Chem. Solids 35, 931 (1974).

59. J.L. Jacquemin and G. Bordure, J. Phys. Chem. Solids 36, 1081 (1975).

60. F. Simonis, M.v.d. Leij, and C.J. Hoogendoorn, Sol. Energy Mater. 1, 221 (1979).

61. R.L. Weiher, and R.P. Ley, J.Appl.Phys. 37, 299 (1966).

62. V.I. Fistul, and V.M. Vainshtein, Sov.Phys. Solid State 8, 2769 (1967).

63. J.H.W. DeWit, J. Solid State Chem. 8, 142 (1973).

64. A.J. Steckl, and G. Mohammed, J.Appl.Phys. 51, 3890(1980).

65. J.L. Vossen, RCA Rev. 32, 269 (1971).

66. G. Haacke, W.E. Mealmaker, and L.A. Siegel, Thin Solid Films 55, 67 (1978).

67. G. Haacke, Proc. Soc. Photo-Opt. Instrum. Eng. 324, 10 (1982).

68. G. Heiland, E. Mollow, and F. Stockmann, Solid State Phys. 8, 193 (1959).

69. L.B. Valdes, Proc. IRE 42, 420 (1954).

70. R.L. Weiher, and R.P. Ley, J.Appl.Phys. 37, 299 (1966).

71. Standard X-ray diffraction data : for powder sample: ASTM 13-111 for SnO(O); ASTM 5-0467 for SnO_2; ASTM 5-0565 for Si; ASTM 11-694 for Sb_2O_4; ASTM 11-690 for Sb_2O_5;etc.

72. K. Ishiguro, T. Sasaki, T. Arai and I. Imai, J.Phys. Soc. Jpn. 13, 296 (1958).

73. I. Viscrian, and V. Georgescu, Thin Solid Films 3, R17 (1969).

74. W.M. Fiest, S.R. Steele, and D.W. Ready, in 'Physics of thin films' (G. Hass and R.E. Thun eds), vol. 5, p.237, Academic Press, New York (1969).

75. A. Fischer, Z. Naturforsch A9, 508 (1954).

76. S.P. Lyashenko and V.K. Miloslavskii, Opt. Spectros (USSR) 19, 55 (1965).

77. D. Elliott, D.L. Zellmer, and H.A. Laitinen, J.Electrochem. Soc. 117, 1343 (1970).

78. A.R. Peaker, and B. Horsley, Rev. Sci. Instrum. 42, 1825 (1971).

79. J.C. Manifacier, L. Szepessy, J.F. Bresse, M. Perotin, and R. Stuck, Mat. Res. Bull. 14, 163 (1979).

80. H. Haneko and K. Miyake, J.Appl.Phys. 53, 3629 (1982).

81. R. Groth and E. Kauer, Philips Tech. Rev. 26, 105 (1965).

82. H. Iida, N. Shiba, T. Mishuku, A. Ito, H. Karasawa, M. Yamanaka, and Y. Hayashi, IEEE Electron Dev. Letters EDL-3, 114 (1982).

83. J. Kane, H.P. Schweizer, and W. Kern, J. Electrochem. Soc. 122, 1144 (1975).

CHAPTER 3

ELECTRICAL CHARACTERIZATION OF CHEMICAL VAPOR DEPOSITED SnO_2-Si HETEROJUNCTIONS

3.1 INTRODUCTION

Tin oxide and indium oxide films not only possess high optical transparency and high electrical conductivity, but have the ability to form very high barriers on semiconductors such as silicon. This makes them very attractive for opto-electronic applications such as solar cells and imaging devices.

A large number of techniques as discussed in Section 2.2 can be employed to deposit thin layers of transparent conductors. Some of these, as spray hydrolysis, have been routinely carried out to prepare layers of tin oxide or indium oxide for less demanding applications such as conductive coatings on aircraft wind shields etc. More sophisticated electronic device applications such as SnO_2 (or In_2O_3)-Si heterojunction solar cells or In_2O_3 (or SnO_2)-SiO_x-Si solid state imaging devices, require not only adequate transparency and conductivity, but also high barriers and good interface properties, and chemical stability.

Spray hydrolysis has been widely employed for solar cell fabrication as it can economically deposit layers over large

areas and lends itself easily to automation. Efficiencies exceeding 14% have been reported for spray deposited SnO_2-Si and In_2O_3-Si solar cells [1,2]. However, problems with uniformity of films and reproducibility are frequently encountered. The usual chemical vapor deposition in a standard tube furnace employing the same hydrolytic reaction as in case of spray deposition can lead to more uniform and reproducible films and is likely to be more suitable for electronic device applications.

The solar cell properties of SnO_2 (or In_2O_3)-Si heterojunctions prepared by various techniques have been studied by many investigators [1-12]. An interesting feature that has been observed in case of SnO_2(or In_2O_3)-nSi heterojunction solar cells, prepared by spray hydrolysis, is their consistently high open-circuit voltage (0.5 V or above), but the fill factors have been generally low, resulting in low efficiency solar cells [3,4]. High open-circuit voltage and very good fill factor can be obtained in a heterojunction with high barrier, if thermionic emission or minority carrier injection play a dominant role in carrier transport mechanism. Other transport processes result in undesired diode current component which is generally responsible for poor fill factor. The study of carrier transport mechanism across the barrier and the factors affecting the same become important to identify the origin of undesired diode current component and minimize the same in order to enhance the efficiency of solar cells.

Only a few investigators have attempted the identification of predominant carrier transport processes across SnO_2 (or In_2O_3)-Si heterojunctions [3-8]. Some of them [4-6] seem to have arrived at doubtful conclusions due to incomplete investigations. Maruska et al have studied optical and thermal degradation of spray deposited SnO_2-Si and In_2O_3-Si solar cells and have attempted to explain these degradations from the change in current voltage characteristics of the diode [9]. The basic mechanisms such as carrier transport across the heterojunction, dependence of the heterojunction barrier and transport process on various interface parameters such as traps, and the physical/chemical origin of traps therefore remain to be examined in detail and understood well. Such studies have not been reported so far on chemical vapor deposited SiO_2 (or In_2O_3)-Si heterojunctions. Since the basic hydrolytic reactions and the reagents used in spray and CVD methods are same, such a study can be helpful in determining the superiority of one process over the other.

The present work was mainly aimed at : (i) preparing a set of reproducible SnO_2-nSi heterojunctions by chemical vapor deposition using hydrolytic reaction in a standard tube furnace with and without antimony doping; (ii) examining the mechanism of carrier transport across the heterojunction at room temperature and above; and (iii) investigating the presence and influence of traps and defects on the heterojunction barrier height and the transport process.

3.2 THEORETICAL DISCUSSION

3.2.1 Current Transport Processes in Surface Barrier Devices

Heterojunctions between silicon and transparent conductors such as tin oxide or indium oxide should basically behave as surface barrier devices since the energy bands in transparent conductors are generally assumed to be flat due to their high conductivity/degeneracy. This assumption seems to be correct since the capacitance-voltage characteristics of transparent conductor-oxide-silicon (TCOS) structure are found to be exactly similar to those of the MOS capacitor enabling interface investigation using TCOS structures [13]. For all practical purposes the space charge layer therefore lies entirely in silicon. The heterojunction behaves like a Schottky barrier with thin interfacial layer in many respects, except for the fact that in case of a metal as the barrier forming layer a continum of states exist in the bulk metal, where as in case of transparent conductor as the barrier forming layer a very wide bandgap exists.

Figure 3.1 depicts the energy band diagram of an n-type -Si-SiO_x-SnO_2 heterojunction under a moderate forward bias. The possible mechanisms of carrier transport across such a barrier are also illustrated in this figure. These are [3,14,15] :

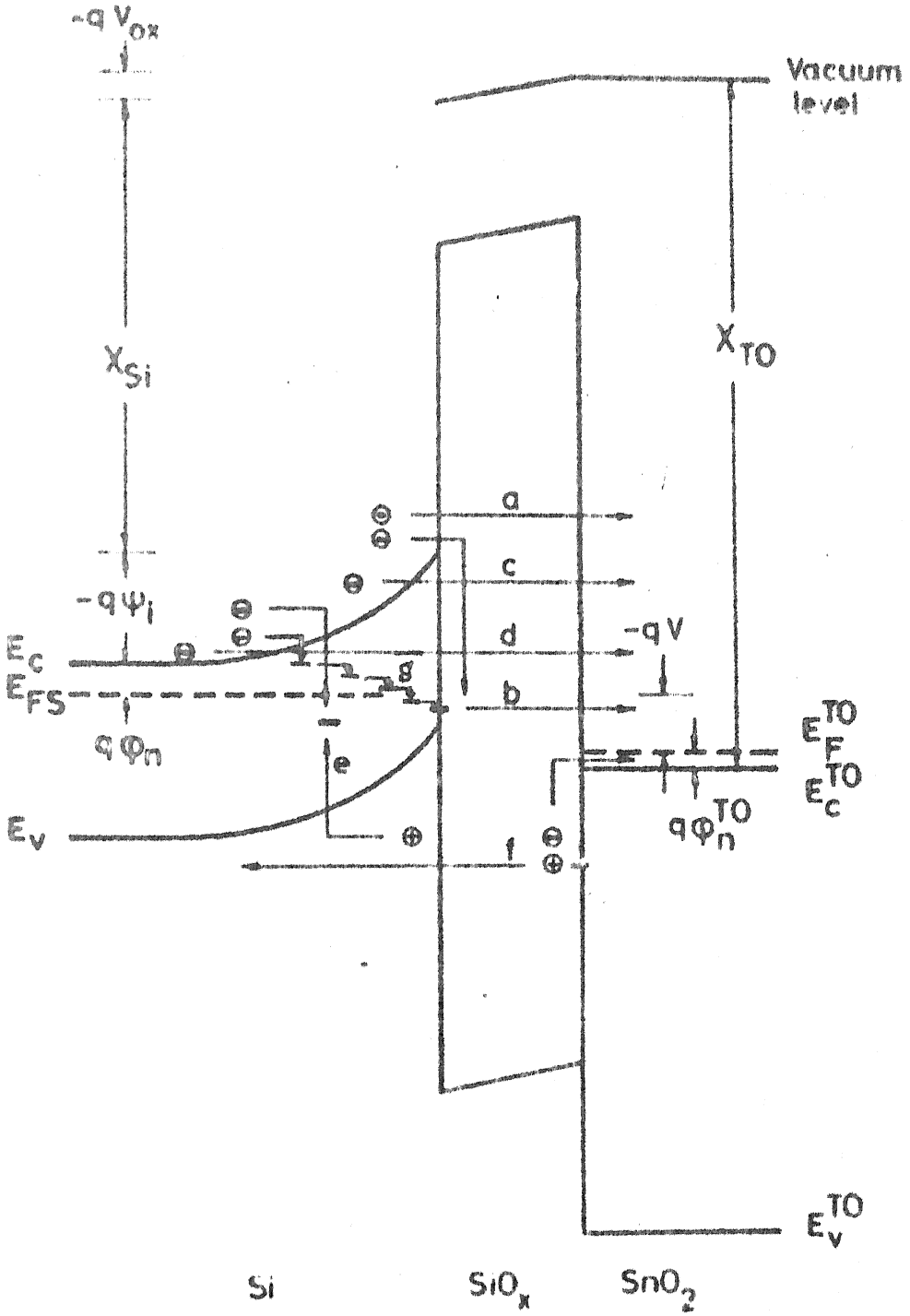


Figure 3.1 Energy band diagram of n-Si/SiO_x/SnO_2 heterojunction, at a forward bias, illustrating various mechanisms of carrier transport across the silicon barrier. Process a is thermionic emission, process b is interface recombination-tunneling, process c is thermionic field emission, process d is field emission, process e is recombination, process f is minority carrier injection, and process g is multistep tunneling

thermionic emission (process a),
recombination-tunneling via interface states (process b),
thermionic field emission (process c),
field emission (process d),
recombination-generation in the space charge layer (process e),
minority carrier injection (process f), and
trap assisted multistep tunneling (process g).

The effect of the oxide barrier on the above processes can generally be represented by means of an oxide transmission coefficient [14-17]. More than one mechanism can contribute to the diode current J , and which mechanism dominates over others depends upon the device temperature, T, the device voltage, V , the surface barrier height, ϕ_b, the silicon doping density, N, and densities of interface states, N_{is}, and traps, N_t, in the space charge layer. The current-voltage characteristic of a surface barrier device is therefore the most difficult of all measured electrical characteristics to interpret. The individual transport processes are discussed below.

Thermionic emission (process a) :

The thermionic emission theory was proposed by Bethe and has been discussed in texts [14]. In this process the carriers with sufficient kinetic energy to raise their energy level up to barrier height get emitted from the semiconductor to metal (or transparent conductor). The current-voltage

relationship is given by the expression :

$$J_t = J_{to} \left[\exp\left(\frac{qV}{kT}\right)-1\right] \qquad (3.1)$$

where J_t is the diode current density due to thermionic emission, J_{to} is the reverse saturation current density, V is the applied bias, q is electronic charge, k is Boltzmann's constant and T is device temperature. J_{to} is related to the barrier height ϕ_b through the expression :

$$J_{to} = A^* T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \qquad (3.2)$$

where A^* is effective Richardson constant.

Equation (3.1) predicts that at any temperature for $V > \frac{3kT}{q}$, ln J_t vs V will be a straight line with unity slope. J_{to} will be given by the intercept of this straight line with current axis at V = o. Equation (3.2) predicts the dependence of J_{to} on barrier height and temperature. If the barrier height is large, the thermionic emission current, J_t, will be small due to small J_{to}. The barrier height can be found experimentally by measuring J_t vs V characteristics at different temperatures and determining J_{to} at each temperature. Equation (3.2) suggests that a plot of ln (J_{to}/T^2) vs $\frac{1}{T}$ should be a straight line whose slope will give the barrier height, ϕ_b. Such a plot is called activation energy plot. The activation energy plot will be linear if barrier height,

ϕ_b, is constant with temperature, T.

Taking into account the image force lowering of the barrier, $\Delta\phi$, Equation (3.1) can be rewritten as [18] :

$$J_t = A^* T^2 \exp(-\frac{q\phi_b}{kT}) \left[\exp\{\frac{q(V+\Delta\phi)}{kT}\} - 1\right] \qquad (3.3)$$

where $\Delta\phi$ is the image force lowering. Since the image force lowering and A^* are both voltage dependent functions, the diode current-voltage characteristic is found to be represented more appropriately by the expression [18] :

$$J_t = J_{to} \left[\exp(\frac{qV}{nkT}) - 1\right] \qquad (3.4)$$

where n is a constant greater than unity and is temperature independent. n is called diode ideality factor. Equation (3.4) suggests that ln J_t vs V plot will be a straight line with a slope greater than unity. It has been found that for nearly ideal diodes, the value of n lies between 1 and 1.1 which can be accounted for by the image force lowering [18].

Recombination -- tunneling via interface states(process b) :

The semiconductor-insulator interface always contains energy states in the forbidden energy gap. The density of these states, N_{is}, depends on various factors. If the density of these states is large, they can assist in carrier transport due to recombination-tunneling, process b, shown in Figure 3.1 [15]. The transition of carriers from silicon majority

carrier band into the interface state takes place due to recombination-generation process and these carriers then tunnel through the oxide causing a diode current J_{rt} to flow, which is given by [15] :

$$J_{rt} = \int_{E_v}^{E_c} \frac{N_{is}(E)\,(f_s - f_m)}{\tau_T}\, dE \qquad (3.5)$$

In this expression J_{rt} is current due to recombination-tunneling process, N_{is} is the density of states, E_c is energy of bottom of conduction band, E_v is energy of top of valence band, τ_T is the oxide tunneling time constant, and f_s and f_m are bulk silicon and metal occupancy functions, respectively. The tunneling time constant is given by

$$\tau_T = B\, e^{\alpha t_{ox}} \qquad (3.6)$$

where B is a constant, t_{ox} is oxide thickness and α is a function of oxide barrier. The current density increases with density of states and is controlled by oxide tunneling time constant which increases with oxide thickness and oxide barrier.

The recombination-tunneling current via interface states J_{rt}, results in a nonlinear ln J_{rt} vs V characteristic (cf. Equation 3.5).

Thermionic-field emission (process c) :

Thermionic emission requires electrons with energies above the top of the barrier. However, under certain conditions the

carriers with energies below the top of the barrier may penetrate the barrier due to quantum mechanical tunneling [14]. This is referred to as thermionic-field emission and is shown as process c in Figure 3.1. The tunneling probability depends on the height and the width of the barrier. Presence of high electric field across the barrier, as in case of degenerate semiconductors or Schottky barriers without guard rings, reduces barrier width. At an intermediate temperature, the electrons are excited to higher energies and the tunneling probability increases considerably as the electrons encounter a thinner and lower barrier. The number of excited electrons however decreases rapidly with increasing energy level at any temperature and hence there is an optimal energy level, the electrons from which will contribute maximum to the current. At a high enough temperature (room temperature) most of the electrons may cross the barrier due to thermionic emission. Thermionic-field emission therefore plays an important role at intermediate temperatures, in degenerate semiconductors, and in the presence of high electric field such as encountered in Schottky barriers without guard ring.

The theory of thermionic-emission has been developed by Padovani and Stratton [19]. It leads to an exponential current vs voltage characteristics, for $V/V_o > 3$, given by expression [14,20] :

$$J_{tf} = J_{tfo} \exp(V/V_o) \qquad (3.7)$$

where J_{tf} is current due to thermionic field emission, J_{tfo} is the corresponding reverse saturation current, and V_o is a parameter which plays an important role in tunneling theory. V_o is given by :

$$V_o = V_{oo} \operatorname{Coth}(q\, V_{oo}/kT) \qquad (3.8)$$

V_{oo} is the diffusion potential of a Schottky barrier such that the transmission probability of an electron with energy coinciding with the bottom of the conduction band at the edge of the depletion layer is equal to e^{-1} [14]. The ratio kT/qV_{oo} is a measure of relative importance of thermionic emission and tunneling. $kT >> qV_{oo}$ leads to thermionic emission, $kT \sim qV_{oo}$ gives rise to thermionic-field emission, while $kT << qV_{oo}$ results in field emission [14]. V_{oo} is a constant depending on doping density, effective mass of electron and permittivity of semiconductor. It is given by

$$V_{oo} = \frac{\hbar}{2} \left[\frac{N}{m_e^* \varepsilon_s}\right]^{1/2} \qquad (3.9)$$

where $\hbar$ is Planks constant divided by 2π, N is doping density, m_e^* is effective mass of electrons in semiconductor and ε_s is semiconductor permittivity.

If we compare Equation (3.7) with Equation (3.4), we get

$$V_o = \frac{nkT}{q} \tag{3.10}$$

Equation (3.7) reveals that ln T_{tf} vs V will still be a linear curve whose slope will give V_o (or nT). Equation (3.8) however indicates that V_o is a nonlinear function of T and hence nT will also be a nonlinear function of T. It has been found that in case of thermionic-field emission $\ln(J_{tfo}/T^2)$ vs 1/T does not give a good straight line. In fact $\ln(J_{tfo}/T^2)$ vs 1/nT gives a straight line [20].

Field-emission (process d) :

Field-emission, shown as process d in Figure 3.1,becomes important at very low temperatures and in highly degenerate semiconductors where the electrical field makes barrier thin enough to allow quantum-mechanical tunneling of electrons at Fermi level. As mentioned above the theory of quantum mechanical tunneling of Padovani et al [19] explains both the thermionic-field emission and the field emission. Field emission becomes important at a temperature when $kT \ll qV_{oo}$ [14]. In such a case Equation (3.8) reduces to

$$V_o = V_{oo} = \frac{\hbar}{2}\left[\frac{N}{m_e^* \varepsilon_s}\right]^{1/2} \tag{3.11}$$

This indicates that though the ln J_f vs V plot , where J_f is diode current due to field emission, will still be a straight line giving V_o from its slope. The value of V_o will be a constant and temperature independent. ln J_f vs V plots at different temperatures will have the same slope. This has been found correct experimentally also [20].

Recombination-generation in the space charge layer (process e) :

Recombination-generation in the space charge layer contributes to diode current via localized centres and the centres near the mid gap have been found to be most effective [14]. The recombination current also gives rise to an exponential current-voltage characteristic, approximately given by [14] :

$$J_r = J_{ro} \{ \exp \left(\frac{qV}{2kT}\right) - 1 \} \qquad (3.12)$$

where J_r is diode current due to recombination generation, and J_{ro} is the reverse saturation current which is inversely proportionate to the life time in depletion region.

$$J_{ro} = \frac{qn_i W}{2 \tau_r} \qquad (3.13)$$

where n_i is the intrinsic electron concentration, W is depletion layer width and τ_r is the lifetime in depletion region. Equation (3.12) shows that ln J_r vs V plot will be a straight line with n = 2. Since n_i is proportional to exp $(-\frac{E_g}{2kT})$, where E_g is semiconductor band gap, the activation energy plot

of ln J_{ro} vs $\frac{1}{T}$ will give an activation energy of $E_g/2$. The recombination current component is generally found in most of the devices. The ratio of thermionic current (J_t) to recombination current (J_r) using Equations (3.1),(3.2),(3.12) and (3.13) comes out to be proportional to :

$$\tau_r \exp[-q(2\phi_b - V - E_g)/2kT]$$

This clearly shows that recombination component becomes important at low voltages, high barrier, low temperature and low minority carrier life time [14].

Presence of recombination current generally causes departure from pure thermionic emission characteristics is a Schottky diode. This may result in ideality factor n between 1 and 2. In such samples the activation energy plot is likely to give two activation energies,

(i) equal to ϕ_b at high temperatures resulting from thermionic emission, and

(ii) equal to approx. $E_g/2$ at low temperatures resulting from recombination current [14]. Since recombination component is more important at lower temperatures while thermionic emission at higher temperatures, the current-voltage characteristics of a diode in which both are dominant in different regions may give temperature dependent n,which decreases as temperature is increased and finally saturates when only thermionic emission dominates.

Minority-carrier injection (process f) :

In case of barrier height on n type material to be greater than $E_g/2$, which is generally obtained in case of SnO_2-nSi heterojunctions, minority carrier (hole) injection (process f in Figure 3.1) may become the dominant carrier transport mechanism. In case of very high barriers, the semiconductor interface may become inverted resulting in high density of minority carriers. These then diffuse to the neutral region of semiconductor under forward bias. This is called minority carrier injection or diffusion current and is similar to p-n junction current. From p-n junction theory, this current is given by [14] :

$$J_h = \frac{qDn_i^2}{L.N} [\exp(\frac{qV}{kT})-1] = J_{ho}[\exp(\frac{qV}{kT})-1] \qquad (3.14)$$

where J_h is diode current due to minority carrier injection, D is minority carrier diffusion constant, L is minority carrier diffusion , length, and J_{ho} is saturation current due to minority carrier injection.

It may be mentioned here that minority carrier injection in case of SnO_2-nSi heterojunctions requires suitable states at SnO_2-SiO_2 interface as shown in Figure 3.1. The reverse saturation current in this case, J_{ho}, is given by :

$$J_{ho} = \frac{qDn_i^2}{L.N} = \frac{qD}{L.N} N_e N_v \exp[-E_g/kT] \qquad (3.15)$$

where N_c and N_v are effective density of states in conduction and valence bands respectively.

The above Equation (3.14) indicates that ln J_h vs V will be a straight line with unity slope. Since $N_c.N_v$ varies as T^3 with temperature, the variation of J_{ho} with temperature will be governed by the exponential term. As temperature increases, E_g decreases and hence J_{ho} will increase more rapidly compared to J_{to} given by Equation (3.2). The activation energy plot may give very slight nonlinearity due to variation of E_g with temperature. The slope of the activation plot will give E_g.

Trap-assisted multistep tunneling (process g) :

Riben et al [21] observed that the temperature dependence of current-voltage characteristics of n Ge-p GaAs heterojunctions could not be explained with any of the existing theories of thermionic emission or diffusion. The main differences were (i) the theory predicted slope of ln J vs V curve to change about 4 times as temperature is reduced from 296°K to 77°K while their results indicated practically the same slope up to 0.7 V, (ii) theory predicted a change in current magnitude of about 16 orders but experiments showed only 6 orders of magnitude change as temp was brought down from 296°K to 77°K, (iii) the currents (forward as well as reverse) predicted by theory were always less than those

obtained experimentally, and (iv) ln J_o vs T was found to be a straight line against ln J_o vs $\frac{1}{T}$ expected theoretically, where J_o is diode saturation current. These led Riben et al [21,22] to propose tap assisted multistep tunneling model in which electrons cross the depletion region due to tunneling via traps employing a staircase path shown as process g in Figure 3.1. The forward current was explained by multistep tunneling while reverse current was explained in terms of Zener tunneling. The forward current in this case, J_{mt}, can be expressed as [23] :

$$J_{mt} = B\ N_t\ \exp[-\alpha\Theta^{1/2}(\Psi_i^o - V_s)] \qquad (3.16)$$

where B is a constant including oxide transmission coefficient N_t is the density of traps in depletion region, Ψ_i^o is zero bias silicon band bending (diffusion potential), V_s is the fraction of applied voltage appearing at semiconductor. α is a function of substrate doping and varies inversely as square root of doping. Θ is defined by $E_t = \Theta(\Psi_i^o - V)$ where E_t is the average energy barrier that the electrons tunnel through. Equation (3.16) indicates that this current component is proportional to density of traps. Also, as doping density increases, α decreases, and the current increases. Also as E_t decreases (due to large trap levels in staircase path), the current increases. The behaviour of all the devices involving multistep tunneling have been shown to follow the following empirical relation [22,23]:

$$J_{mt} = J_{mto} \exp(AV) \exp(BT) \qquad (3.17)$$

where A and B are constants essentially independent of voltage and temperature and J_{mto} is diode saturation current due to multistep tunneling. A is found to be relatively insensitive to the temperature variations [22,23]. A can therefore be estimated from the slope of ln J_{mt} vs V curve at any fixed temperature and B from ln J_{mt} vs T at any fixed voltage (say V = o). These values of A and B will be good as first approximation, neglecting their dependence on temperature and voltage respectively. Riben et al [22] found A to be of the order of 20 to 30 V^{-1} and B in the range of 0.04 to 0.07 $^{o}K^{-1}$. The multistep tunneling theory proposed by Riben et al [21,22] for nGe-p GaAs was found to explain J-V characteristics of other heterojunctions like pGe-nSi and pGe-nGaAs at intermediate and high voltage regions though low voltage regions exhibited recombination-generation currents [23]. Since the slope of ln J_{mt} vs V remains same with temperature, if implies that in case of multistep tunneling process, n.T should be relatively temperature independent.

Evidence of trap-assisted multistep tunneling based on the above discussions have also been found in surface barrier devices like spray deposited In_2O_3-Si heterojunction [3,24], MOS diodes on poly Si [24,25], and Sn-doped SnO_2-Si heterojunction under present investigation [26].

3.2.2 Identification of Current Transport Process

Identification of the most dominant current transport mechanism in any particular diode merely on the basis of current-voltage characteristics is therefore very difficult and it often resulted in doubtful conclusions in the reported literature. For example, exponential J vs V characteristic is generally attributed to either thermionic emission or minority carrier injection even if the diode quality factor n is much larger than unity [4]. However, measurement of current-voltage (J-V) characteristics and high frequency capacitance-voltage (C-V) characteristics at various temperatures can provide useful information. From ln J vs V characteristics the values of ideality factor, n, and saturation current, J_o, can be obtained at different temperatures. High frequency $\frac{1}{C^2}$ vs V characteristics (linear) at these temperatures can give the doping density from the slope (and hence Fermi potential, ϕ_F , from majority carrier band edge) and zero bias silicon band bending, Ψ_i^o, from the intercept to the voltage axis. The total barrier height, $\Psi_i^o + \phi_F$, can therefore be calculated at each temperature from $\frac{1}{C^2}$ vs V plots. If $\frac{1}{C^2}$ vs V gives more than one slope, it indicates the possibility of presence of deep level traps and the low frequency $\frac{1}{C^2}$ vs V characteristics can then be used to get more information about these traps [26]. This has been discussed in detail in Section 3.2.3. In case of sufficiently thick oxides where small signal admittance-voltage characteri-

density can be obtained,which can be helpful in determining the possibility of recombination-tunneling via interface states [15,16].

The following procedure can be adapted for identification of carrier transport mechanism once the above mentioned information is obtained from J vs V and C vs V characteristics at various temperatures :

(i) The recombination-tunneling process via interface states gives rise to nonexponential J vs V curve as discussed earlier, and hence can be neglected if exponential J vs V curve is obtained at room temperature. All the remaining transport processes result in exponential J-V curves but the simultaneous presence of a few of them may result in different slopes of ln J vs V curve in different regions.

(ii) If ln J vs V characteristics remain linear over wide voltage and temperature range with diode quality factor n independent of temperature having a value close to unity, and if ln J_o vs T^{-1} plot is also linear then the dominant process may either be thermionic emission or minority carrier injection. Now if the activation energy obtained from ln J_o vs T^{-1} plot and the barrier height, $\Psi_i^o + \phi_F$, match with each other at each temperature and their value is much different from the bandgap, then thermionic emission is the most likely mechanism. On the otherhand,if the barrier height from $\frac{1}{C^2}$ vs V and activation

energy plots come out to be close to the band gap, thermionic emission and minority carrier injection cannot be differentiated easily. The general belief is that minority carrier injection may dominate in this case. Nielsen [17,27] has suggested that thermionic emission and minority carrier injection can be differentiated from the variation in ln J vs V characteristics with temperature. If these characteristics at two temperatures T_1 and T_2 ($T_2 > T_1$) are studied, then for a constant diode current, the increase in saturation current with temperature is given by [17] :

$$\ln \left[\frac{J_o(T_2)}{J_o(T_1)}\right] = \left(\frac{qV_1}{kT_1} - \frac{qV_2}{kT_2}\right) \qquad (3.18)$$

where V_1 is the voltage giving the same diode current at temperature T_1 and V_2 is the voltage giving the same diode current at temperature T_2. $\ln \frac{J_o(T_2)}{J_o(T_1)}$ can be easily calculated from measured characteristics.

The ratio of diode saturation current at two temperatures, T_2 and T_1, for a minority carrier injection current has been shown theoretically to be [27] :

$$\ln \left[\frac{J_o(T_2)}{J_o(T_1)}\right] = \ln \left[\left(\frac{T_2}{T_1}\right)^{5/2}\right] + \left[\frac{E_G(T_1)}{kT_1} - \frac{E_G(T_2)}{kT_2}\right] \qquad (3.19)$$

Knowing temperatures T_1 and T_2 and calculating $E_G(T)$ at these temperatures, the values of $\ln \left[\frac{J_o(T_2)}{J_o(T_1)}\right]$ calculated using

equation (3.19) and experimentally obtained using equation (3.18) can be compared. If they match then minority carrier injection is the dominant transport process.

(iii) If the diode quality factor n has a value considerably higher than 1 (close to 2), and if $\Psi_i^o + \phi_F$ from $\frac{1}{C^2}$ vs V plot comes out to be high but the activation energy from $\ln J_o$ vs $\frac{1}{T}$ plot comes out to be approximately half the band-gap, then recombination-generation in space charge layer via mid gap traps is likely to be dominant mechanism.

(iv) If the diode quality factor n has a value between 1 and 2 or if ln J vs V has two slopes giving n_1 (low bias) > 1 and n_2 (intermediate bias) ~ 1, and if $\ln J_o$ vs $\frac{1}{T}$ plot gives two activation energies, (a) approximately equal to half the band-gap at low temperatures and (b) equal to barrier heigh, $\Psi_i^o+\phi_F$, obtained from $\frac{1}{C^2}$ vs V plot at high temperatures, then both thermionic emission (or minority carrier injection) and recombination-generation in space charge layer are contributing to diode current. This is a commonly observed feature in Schottky barriers. Recombination-generation plays a dominant role at low bias and low temperatures while thermionic emission (or minority carrier injection) becomes dominant at intermediate bias and high (room) temperatures.

(v) Field emission [14,20] becomes important at very low temperatures and in case of highly degenerate semiconductors. The

current-voltage characteristic may still be exponential but the slope (or n.T.) remains constant with temperature. ln J vs V characteristics therefore show a nearly parallel shift and the effect of temperature is small. Field emission can however be neglected at high (room) temperatures and for non generate semiconductors.

(vi) In case of thermionic field emission, the J-V characteristics will be exponential but the diode ideality factor n and the slope of ln J vs V plot, n.T., will be a nonlinear function of T. The activation energy plot of ln J_o vs $\frac{1}{T}$ will be nonlinear but ln J_o vs $\frac{1}{nT}$ will be linear. Hence, this can be easily distinguished.

(vii) Multistep tunneling also results in exponential J vs V characteristics. However, as mentioned earlier the slope of ln J vs V plot, n.T, remains constant with temperature. As in case of field emission, ln J vs V characteristics will show nearly a parallel shift and the effect of temperature will be smaller compared to that expected due to other mechanisms. The most striking feature of multistep tunneling mechanism is that ln J_o is not a linear function of $\frac{1}{T}$ but is a linear function of T. Multistep tunneling also results in J_o considerably higher than those expected from other mechanisms. Value of A is generally found between 20 and 30 V^{-1} while that of B is found between 0.04 to 0.07 $^oK^{-1}$ [8,21,24].

3.2.3 Effect of Deep Level Traps

Figure 3.2(a) represents the energy band diagram of the silicon space charge layer containing, in addition to the shallow donor levels, a number of deep level traps, under reverse bias condition. Charging/discharging takes place at any particular trap level, when the electron quasi-Fermi level, E^{c}_{FS}, at a point X^{d}_{i}, is in the neighbourhood of a donor trap level, E^{i}_{TD}, and/or the hole quasi-Fermi level, E^{h}_{FS}, at a point X^{a}_{i}, is in the neighbourhood of an acceptor trap level, E^{i}_{TA}. Any charging/discharging adds to the capacitance, irrespective of whether the trap is a donor or an acceptor. When both kinds of traps are present, the resultant slope of C^{-2} vs V plot relates to the sum of the densities of all traps and the shallow dopant. In other words, the slope of C^{-2} vs V plot will not reflect any compensation taking place. The response of a trap, located at a certain point in the space charge layer, to an ac signal, will depend upon a number of factors. As mentioned earlier, the response will be significant only if the relevant quasi-Fermi level is in the vicinity of the trap level. Secondly, there will be an equilibrium frequency, below which the traps will be able to follow the applied ac signal, and above which the traps will not respond to the signal or respond only partly. If there are a number of trap levels distributed over the bandgap, it follows, that at an intermediate frequency, some trap levels will follow the signal, and the others will not.

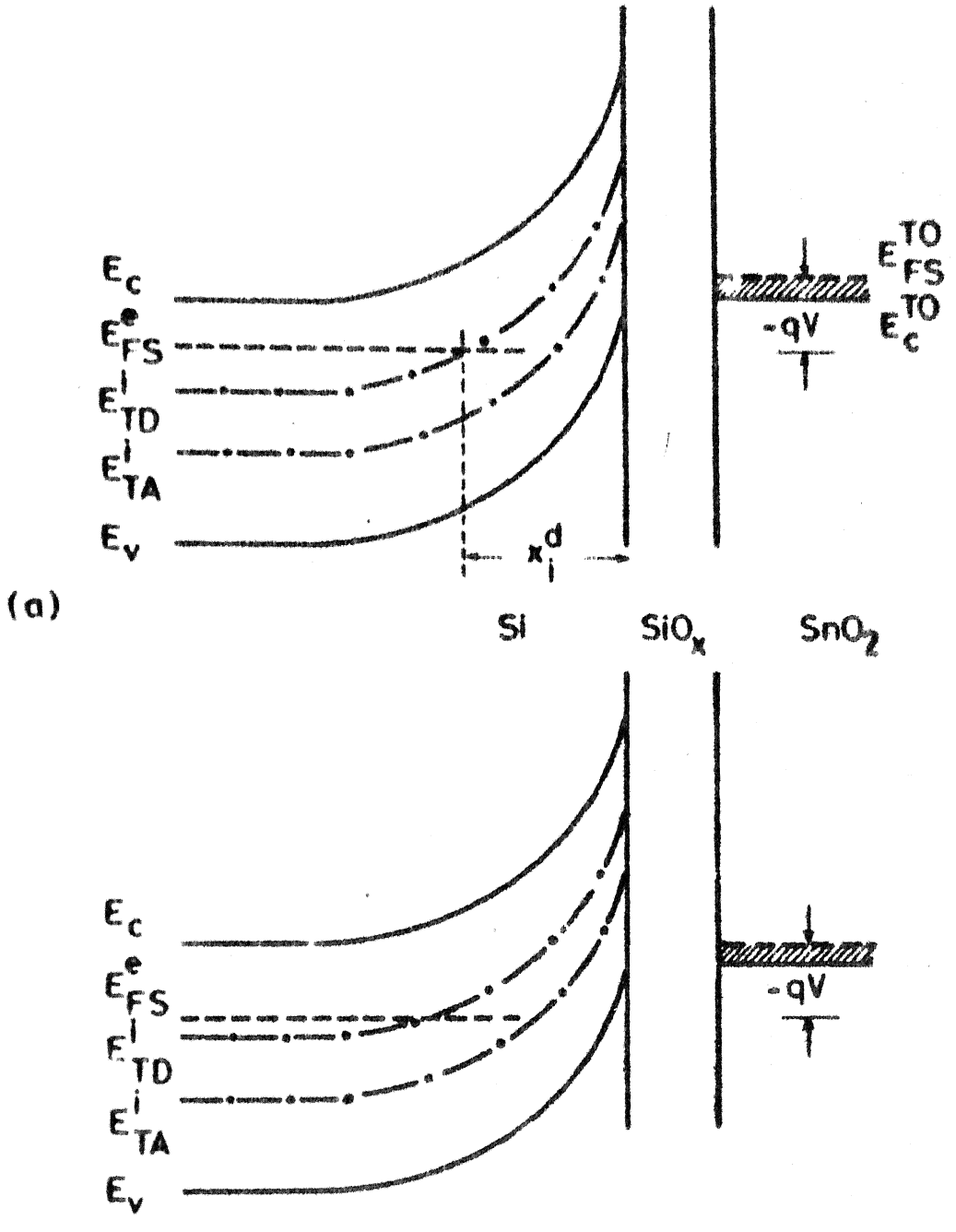


Figure 3.2 Energy band diagram of the silicon space charge layer, containing a number of trap levels, in addition to the shallow donor level, under reverse bias condition: (a) at room temperature, (b) at higher temperature

If the trap densities are uniform over the space charge layer and are comparable to the shallow doping density, then charging/discharging at the traps will influence the space charge capacitance in the following manner. We first consider that the space charge layer contains just one donor trap level, E^i_{TD} of Figure 3.2(a), and assume that it has a density N^i_{TD}, that this trap can completely follow the ac signal, and that the electron quasi-Fermi level is flat up to the silicon surface. If we begin bending the energy bands in silicon downwards (depletion region) from the flat band condition, then, initially the slope of C^{-2} vs V plot will relate only to the donor density N_D, and will not reflect the trap density, N^i_{TD}, until the increasing band-bending brings the trap level in the vicinity of the electron quasi-Fermi level at the silicon surface. For a bias which will increase the band-bending further, the slope of C^{-2} vs V plot will be smaller and will relate to the density $(N_D + N^i_{TD})$. If instead of a single donor trap, a number of donor trap levels are present, and the other assumptions mentioned above remain valid, then each time the electron quasi-Fermi level intersects a new trap level at the interface, the slope of C^{-2} vs V plot will change, become smaller, and will relate to the density $(N_D + \Sigma_i\ N^i_{TD})$, where the sum includes densities of all the donor traps whose levels are higher than E^e_{FS} at the silicon surface. The behavior of C^{-2}-V, however, becomes more complex when a number

of both donor and acceptor trap levels are present, when the quasi-Fermi levels are not constant throughout the space charge layer, and when the ac signal frequency is in the intermediate range, such that only a part of the traps can respond to it.

As the temperature is increased, the bulk Fermi level moves away from the majority carrier band. If one compares the energy band diagram of Figure 3.2(b) to that of Figure 3.2(a), the former representing the situation at a higher temperature, it becomes apparent that, with increasing temperature, a largernumber of trap levels will move above the quasi-Fermi levels at the silicon surface for the same band-bending. Further, the value of silicon band-bending for which all the existing trap levels will move above the quasi-Fermi levels at the silicon surface, will be lower at a higher device temperature. This feature is likely to reflect in the C^{-2} vs V characteristics in the following manner. At lower temperatures, the traps will cause the reverse C^{-2} vs V characteristics to change slope and have a smaller slope with increasing reverse bias, but, above a certain temperature, the reverse characteristics with exhibit a single but smaller slope.

3.3 EXPERIMENTAL DETAILS

3.3.1 Sample Fabrication

Silicon-tin oxide heterojunctions were fabricated on n^+n

epitaxial wafers, obtained from Monsanto Company with (100) surface orientation. The epitaxial layer was 9 microns thick and had a resistivity of about 1.0 Ohm-cm. The wafers were degreased in warm trichloroethylene, in warm acetone, ultrasonically cleaned in acetone, and finally degreased in warm methanol. After degreasing, the wafers were rinsed in deionized water having a resistivity of 12-14 M ohm-cm, etched in HF, and again rinsed in deionized water. All the solvents and acid used were electronic grade. The wafers after rinsing were dried in filtered dry oxygen gas at the mouth of the furnace and immediately introduced into the thermco resistance-heated furnace. Oxidation was carried out in dry oxygen at 1100°C for 30 min at atmospheric pressure. This oxidation was a part of the wafer surface cleaning and the wafers were then etched in HF and rinsed in deionized water. They were then ultrasonically cleaned in acetone, etched in HF and finally rinsed in deionized water. This elaborate wafer cleaning procedure was found necessary to obtain the wafer surface free from any silicon dust which was observed on the wafer surface after wafer scribing and could not be removed by degreasing or ultrasonic cleaning.

Immediately after surface cleaning, the wafers were placed horizontally on a quartz boat with molybdenum mask, having holes of 2-3 mm diameter, on their surface to define the area of the diode. The boat was introduced immediately into

the chemical vapor deposition setup and SnO_2 film was deposited on silicon substrate as discussed in details in Section 2.3. Molten $SnCl_4.5H_2O$ at 93°C and deionized water at 23°C were used as source material for depositing undoped SnO_2 films while antimony doping was carried out with the help of molten $SbCl_3$ source at 93°C. Nitrogen was used as the carrier gas and the substrate temperature was maintained at 300°C. The nitrogen flow rate through the Sn source was typically 550 cc/min, while that through deionized water was 1250 cc/min. In case of doped films, nitrogen gas was bubbled through molten $SbCl_3$ at a rate of 0-40 cc/min. Although the same furnace was used for depositing both undoped and doped tin oxide films, different sets of furnace tubes, boats, masks and other attachments were employed in the two cases. Deposition was typically carried out for about 60 min. An interfacial oxide may have grown on the silicon surface before SnO_2 deposition, however, this oxide was not optimized and its thickness should be less than 20 Å as indicated by C-V measurements. After chemical vapor deposition of tin oxide, the front surface of the devices was masked with Apiezon wax and the oxide layer from the back of the hetero-junction samples was etched in HF and rinsed in deionized water. The Apiezon wax was removed in warm trichloroethylene and the heterojunctions were degreased in warm acetone and in warm methanol. The samples were then introduced into an

oil-free high vacuum system and aluminum was evaporated from a filament source to form back ohmic contact on the silicon substrate. The chamber pressure during evaporation was $1x10^{-5}$ torr. Aluminum of 5N purity was thoroughly degreased before loading into the filament source for evaporation. No metal contact pad was deposited on the tin oxide dots of the heterojunctions.

3.3.2 Electrical Measurements

Electrical measurements were carried out at a number of temperatures in the range of 294-394^{o}K. The samples were placed on a gold plated copper block inside a light and electrically shielded box because of their high sensitivity to light. The temperature of the sample could be varied with a heater built-in to the copper block and the same could be controlled within $\pm$ 0.5^{o}C with the help of temperature controller. The temperature was measured with the help of a chromel-alumel thermocouple. Electrical contact to the semiconductor substrate was made through the copper block on which the sample was placed while contact to the tin oxide dot was made with the help of a gold plated sharp pointed telescopic spring probe mounted on a micromanipulator. The diode current-voltage (I-V) characteristics of the heterojunctions were recorded in dark with the help of a Keithley 191 digital multimeter, a Keithley 610 C electrometer, and a finely adjustable dc power supply. The capacitance-voltage (C-V)

characteristics of the diodes were measured, in dark, for reverse bias, with the help of a General Radio 1616 precision capacitance system, a Keithley 616 digital electrometer, and an adjustable dc power supply. The small ac signal frequency was in the range of 50 kHz to 400 Hz. The area of the diode was carefully measured under Unitron optical microscope.

3.3.3 Data Analysis

The diode current-voltage characteristics at different temperatures were plotted on a semilogarithmic graph resulting in ln I vs V curves. From the linear portion of these curves in intermediate voltage regime, the diode quality factor, n, and from extrapolation of the linear regions, the zero-voltage diode current density intercept J_o were calculated at each temperature of measurement. The current density intercept, J_o was plotted as a function of T^{-1}, and also as a function of T on semilogarithmic graphs, in order to identify the carrier transport mechanism. If ln J_o was a linear function of T^{-1}, the activation energy was calculated from its slope. J_o was also used to calculate equivalent thermionic barrier height, $\phi_b^{eqv.}$, at different temperatures. If ln J_o was a linear function of T, then assuming multistep tunneling as the dominant transport mechanism, the values of constants A and B in Equation (3.17) were calculated.

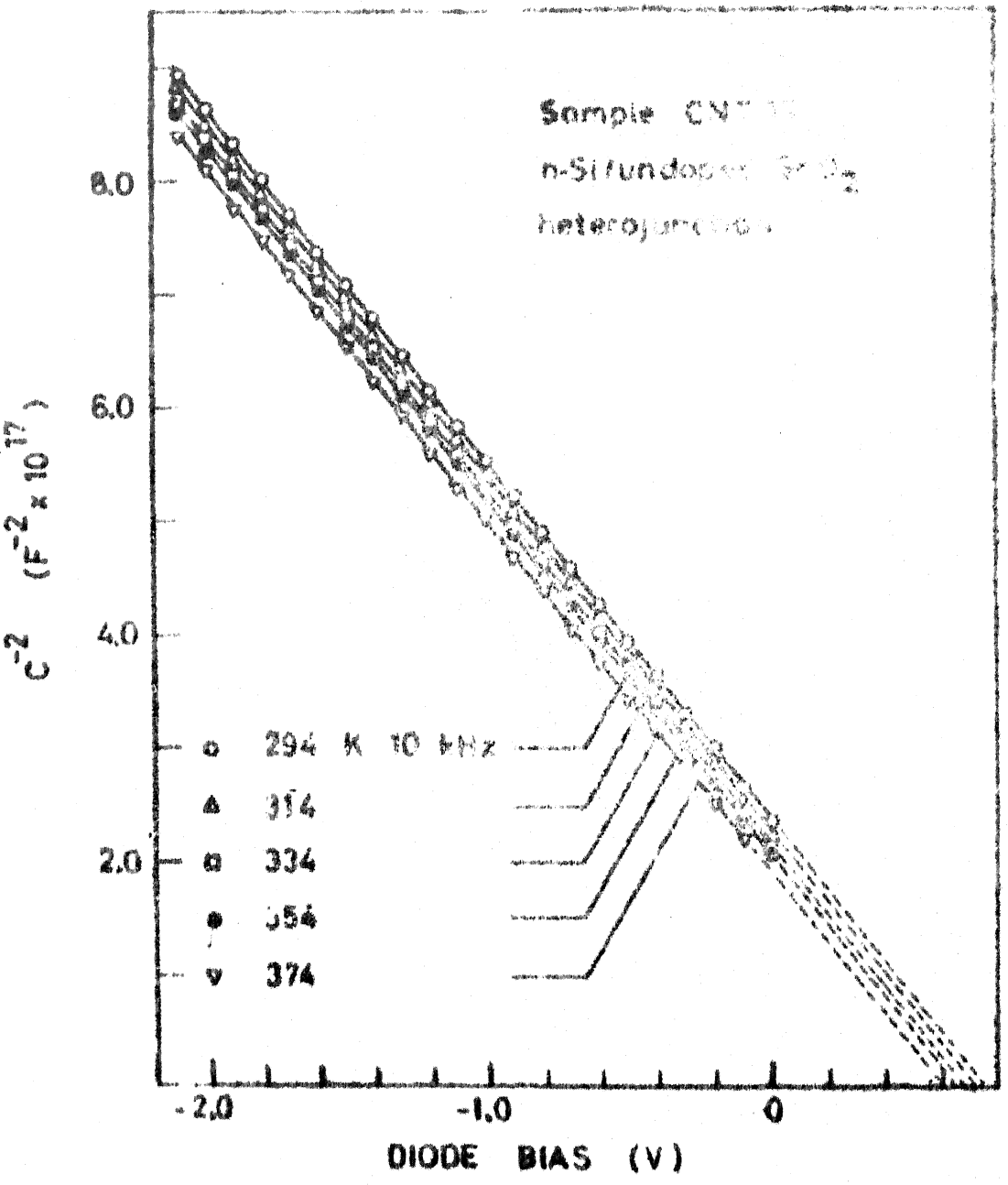


Figure 3.4 Measured 10 kHz C^{-2} vs V characteristics of a typical undoped SnO_2-nSi heterojunction CNT 15 at device temperatures of 294, 314, 334, 354 and 374°K

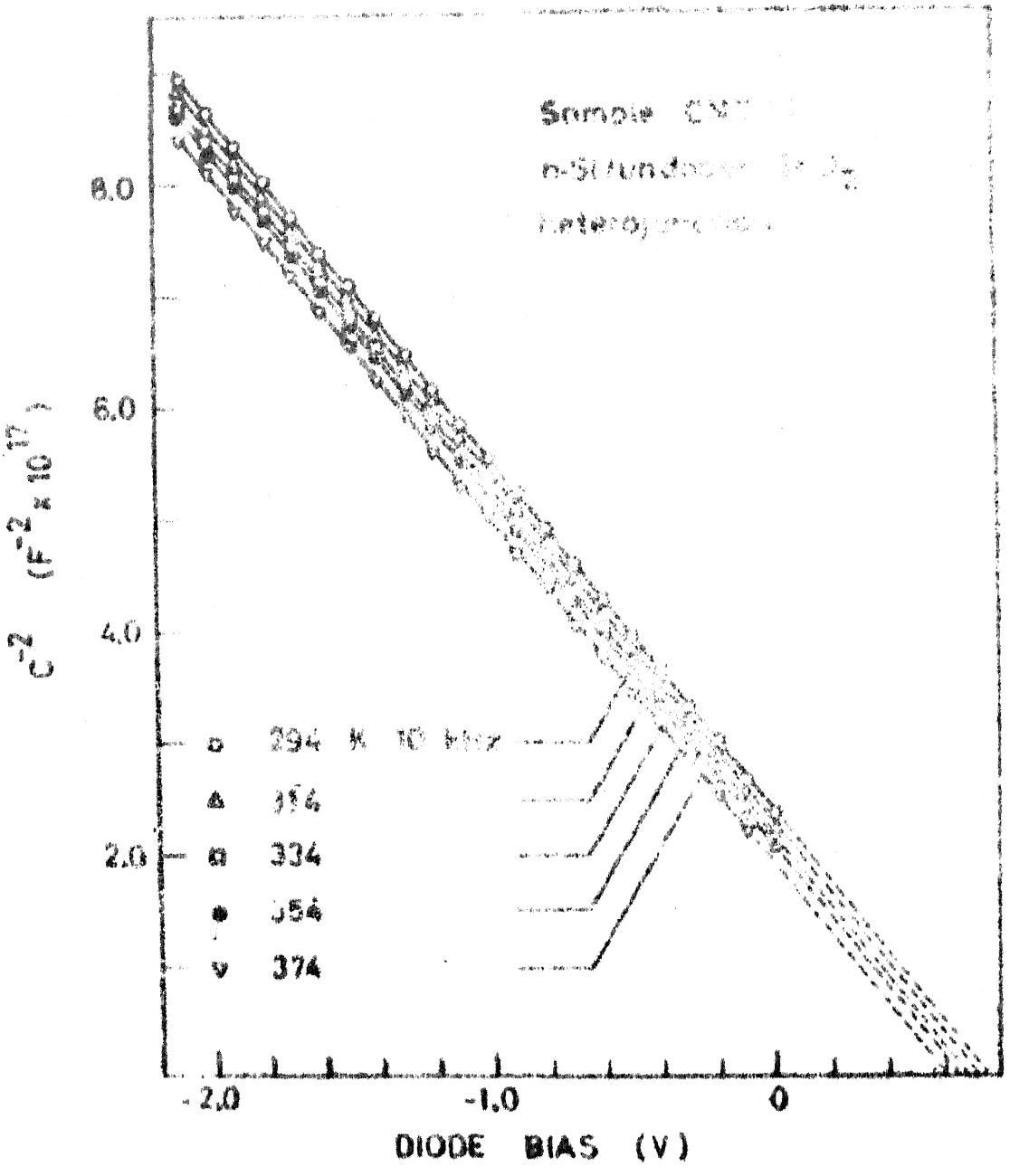


Figure 3.4 Measured 10 kHz C^{-2} vs V characteristics of a typical undoped SnO_2-nSi heterojunction CNT 15 at device temperatures of 294, 314, 334, 354 and 374°K

measured was 10 kHz. At higher frequency the reverse conductance became too high to be balanced on the bridge. The C^{-2} vs V characteristics are also linear at the temperatures of measurement. The experimental data obtained for heterojunction CNT 15 from Figures 3.3 and 3.4, i.e., the zero-bias current density intercept J_o, the ideality factor n, the equivalent thermionic barrier height $\phi_b^{equ.}$, the silicon donor density N_D, the bulk Fermi level ϕ_n, and the zero-bias silicon band-bending Ψ_i^o, have been summarized in Table 3.1. Figure 3.5 illustrates the dependence of ln J_o on T^{-1}, and Figure 3.6 shows the behavior of ln J_o with T.

It appears from Figures 3.5 and 3.6, that for sample CNT 15, ln J_o is more linear with T^{-1} than with T. The activation energy obtained from the slope of ln J_o vs T^{-1} plot came out to be 0.58 eV, which is about half the silicon bandgap. On the other hand, Table 3.1 indicates the uncorrected barrier height, $\phi_b = \Psi_i^o + \phi_n$, obtained from C^{-2}-V characteristics, to be in the range of 0.97 - 0.89 eV, which is much higher than the activation energy of 0.58 eV obtained from Figure 3.5. Further, the thermionic barrier height equivalent, $\phi_b^{eqv.}$, of J_o came out in the range of 0.84 - 0.87 eV, c.f. Table 3.1. These features and the fact that the diode quality factor, n, is in the range of 1.65 - 1.78, would seem to rule out thermionic emission or minority carrier injection to be the likely dominant mechanism of carrier transport across the silicon

Table 3.1 : Experimental data of sample CNT 15 (undoped SnO_2-nSi heterojunction) obtained from measured I-V and C^{-2}-V characteristics. The doping density calculated from the slope of C^{-2}-V plot is : $N_D = 6.0 \times 10^{15}$ cm^{-3}. ϕ_b^{eqv} is thermionic barrier height equivalent calculated from J_o

T (o)	n	J_o (A/cm^2)	ϕ_b^{eqv} (V)	ϕ_n (V)	Ψ_i^o (V)	$\Psi_i^o + \phi_n$ (V)
294	1.65	9.0×10^{-8}	0.84	0.21	0.76	0.97
314	1.67	4.1×10^{-7}	0.84	0.22	0.73	0.95
334	1.70	1.7×10^{-6}	0.85	0.24	0.69	0.93
354	1.74	5.6×10^{-6}	0.86	0.25	0.66	0.91
374	1.78	2.0×10^{-5}	0.87	0.27	0.62	0.89

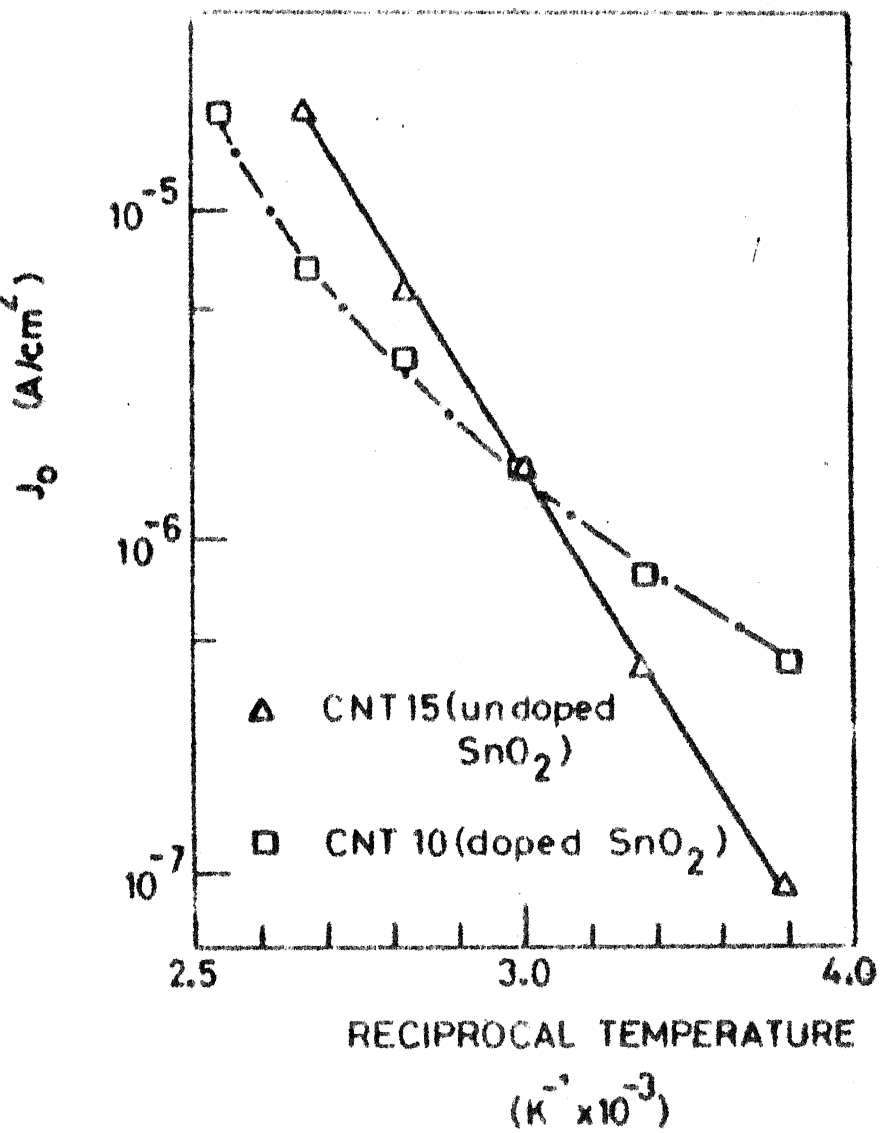


Figure 3.5 Measured J_o vs 1/T, on a semilogarithmic graph, of samples CNT 15 and CNT 10

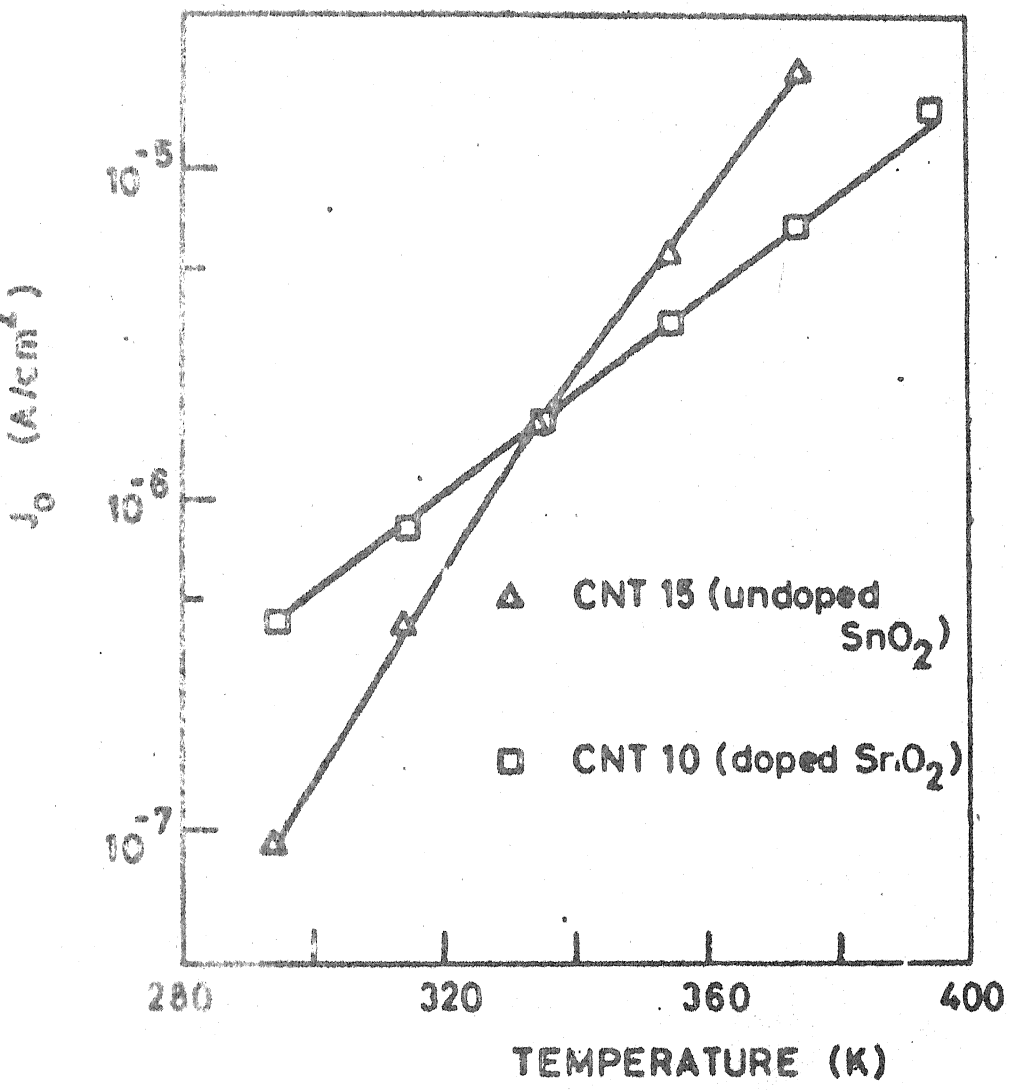


Figure 3.6 Measured J_o vs T, on a semilogarithmic graph, of sample CNT 15 any CNT 10

barrier. The experimental data of sample CNT 15, on the basis of discussion in Section 3.2, on the other hand, indicate the most likely transport mechanism to be recombination-generation in the space charge layer. The effective minority carrier lifetime [28], $\tau_{eff} = q.n_i.W_o/J_o$ (where n_i is the intrinsic carrier density and W_o the zero-bias space charge width), calculated from J_o comes out to be 1.1×10^{-6}S.

The value of $6.0 \times 10^{15} cm^{-3}$ obtained for the doping density from the slopes of the C^{-2} vs V characteristics of Figure 3.4 do not reflect any noticeable change with temperature and is close to the value of 5.0×10^{15} cm^{-3} which corresponds to the bulk resistivity of 1.0 Ohm.cm. The single slope of C^{-2} vs V characteristics indicate that the deep level trap density is small compared to the shallow level donor density, N_D. The decrease in the zero-bias silicon band bending, Ψ_i^o, with increasing temperature, as represented by the measured data of Figure 3.4, can be partially accounted for by the increase in the bulk Fermi level ϕ_n. However, still the sum $(\Psi_i^o + \phi_n)$ is not constant, but decreases with increasing temperature, cf. Table 3.1.

According to the energy level diagram of Figure 3.1, one can obtain for the zero-bias silicon band-bending :

$$\Psi_i^o = [(\chi_{To} - \chi_{Si})/q] - \phi_n - \phi_n^{To} - V_{ox}^o \qquad (3.20)$$

where χ_{TO}, χ_{Si} are tin oxide and silicon electron affinities, respectively, ϕ_n is silicon bulk Fermi level seperation from majority carrier band edge, while ϕ_n^{TO} is tin oxide bulk Fermi potential, and V_{ox}^o is the zero-bias potential across the interfacial SiO_x layer. According to Equation (3.20), if $(\chi_{TO}-\chi_{Si})$ can be considered independent of temperature, then the temperature dependence of Ψ_i^o can be the consequence of change in ϕ_n, ϕ_n^{TO} and V_{ox}^o with temperature :

$$\frac{d\Psi_i^o}{dT} = -\left(\frac{d\phi_n}{dT} + \frac{d\phi_n^{TO}}{dT} + \frac{dV_{ox}^o}{dT}\right) \qquad (3.21)$$

The amount of change of ϕ_n with T is shown in Table 3.1, and $\frac{d\phi_n}{dT}$ is positive. The tin oxide Fermi level at 0^oK is related to its electron concentration, n_e, in the following manner[29]

$$q\phi_{no}^{TO} = (\hbar^2/2m_e^*)(3\pi^2 n_e)^{2/3} \qquad (3.22)$$

where $\hbar = \frac{h}{2\pi}$, h is Planck's constant, and m_e^* effective mass of conduction electrons in tin oxide. ϕ_{no}^{TO} can be calculated if n_e in tin oxide is determined experimentally. The tin oxide Fermi level at a given temperature T is related to ϕ_{no}^{TO} in the following manner [29] :

$$\phi_n^{TO} = \phi_{no}^{TO}\left[1-(\pi^2/12)(kT/\phi_{no}^{TO})^2\right] \qquad (3.23)$$

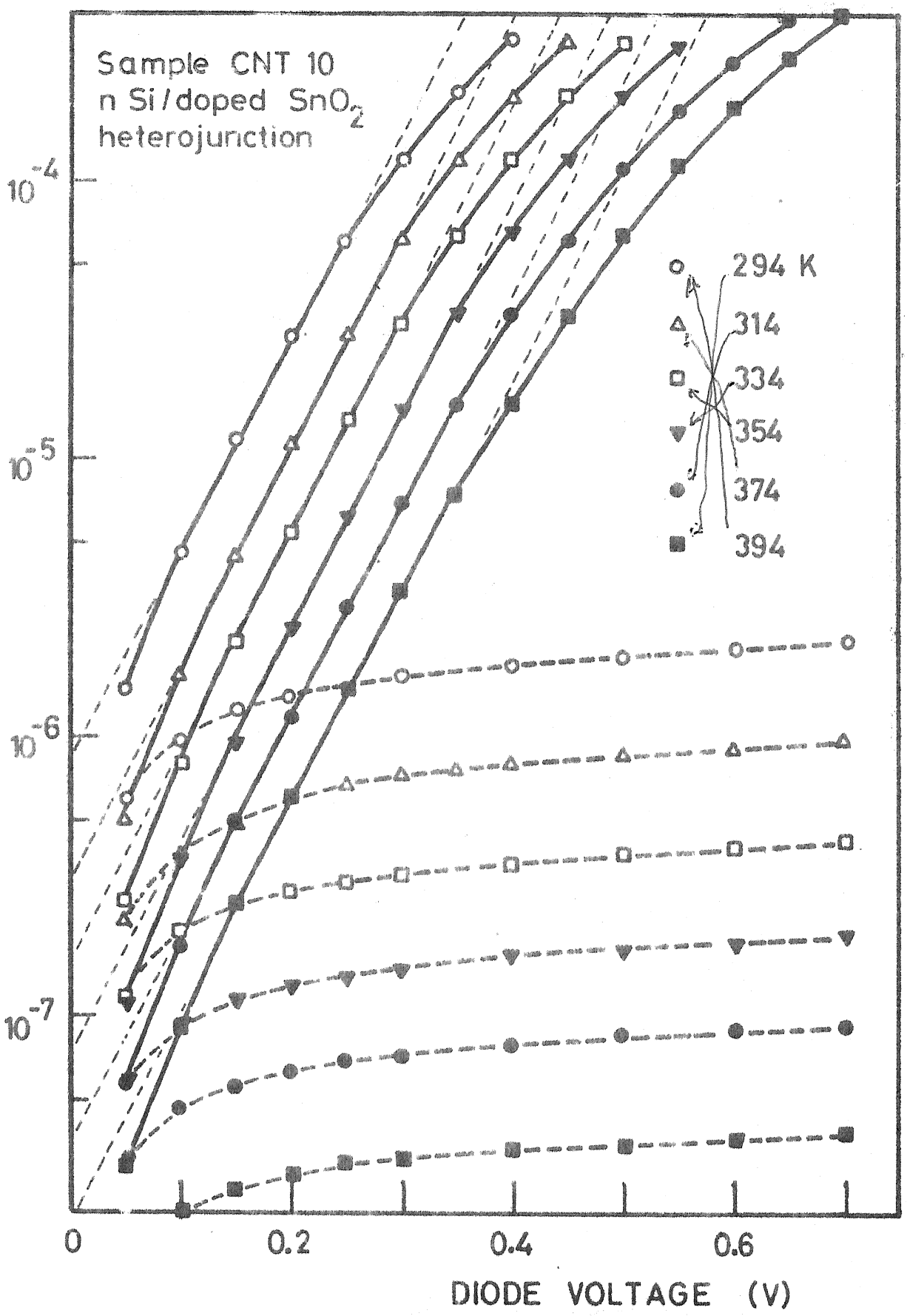
Equation (3.23) indicates that $\frac{d\phi_n^{TO}}{dT}$ is negative. Although one cannot find $\delta\phi_n^{TO}$ unless n_e is determined, a rough

estimate shows that the change in ϕ_n^T over the temperature range 294-374°K would be only a few mV and hence this component can be neglected in Equation (3.21). The third component in Equation (3.21), namely (dV_{ox}^o/dT) can be calculated only if the corresponding change in space charge density δQ_{sc} and in interface charge density δQ_{ic} are known. However, by putting the values of $\delta \Psi_i^o$ and $\delta \phi_n$ from Table 3.1 for the temperature range of 294-374°K, it is estimated that V_{ox}^o increased by about 0.08 V as temperature increased from 294 to 374°K.

3.4.2 Characteristics of Sb Doped SnO_2/n-Si Heterojunctions

Figure 3.7 presents the diode current-voltage characteristics of sample CNT 10, a typical heterojunction between n-Si and antimony-doped tin oxide. These characteristics were measured at device temperature of 294,314,334,354,374 and 394 °K. The C^{-2} vs V characteristics of this sample, measured at the same temperatures, have been depicted in Figure 3.8. For this heterojunction, the highest frequency at which the reverse C-V could be measured was 50 kHz. The experimental data obtained from Figures 3.7 and 3.8 have been summarised in Table 3.2. Figure 3.5 depicts the behavior of ln J_D^o with T^{-1} and Figure 3.6 with T, respectively.

The forward diode current of heterojunction CNT 10, also, is found to be an exponential function of the applied bias in


Sample CNT 10
n Si/doped SnO_2
heterojunction
294 K
314
334
354
374
394
10^{-4}
10^{-5}
10^{-6}
10^{-7}
0
0.2
0.4
0.6
DIODE VOLTAGE (V)

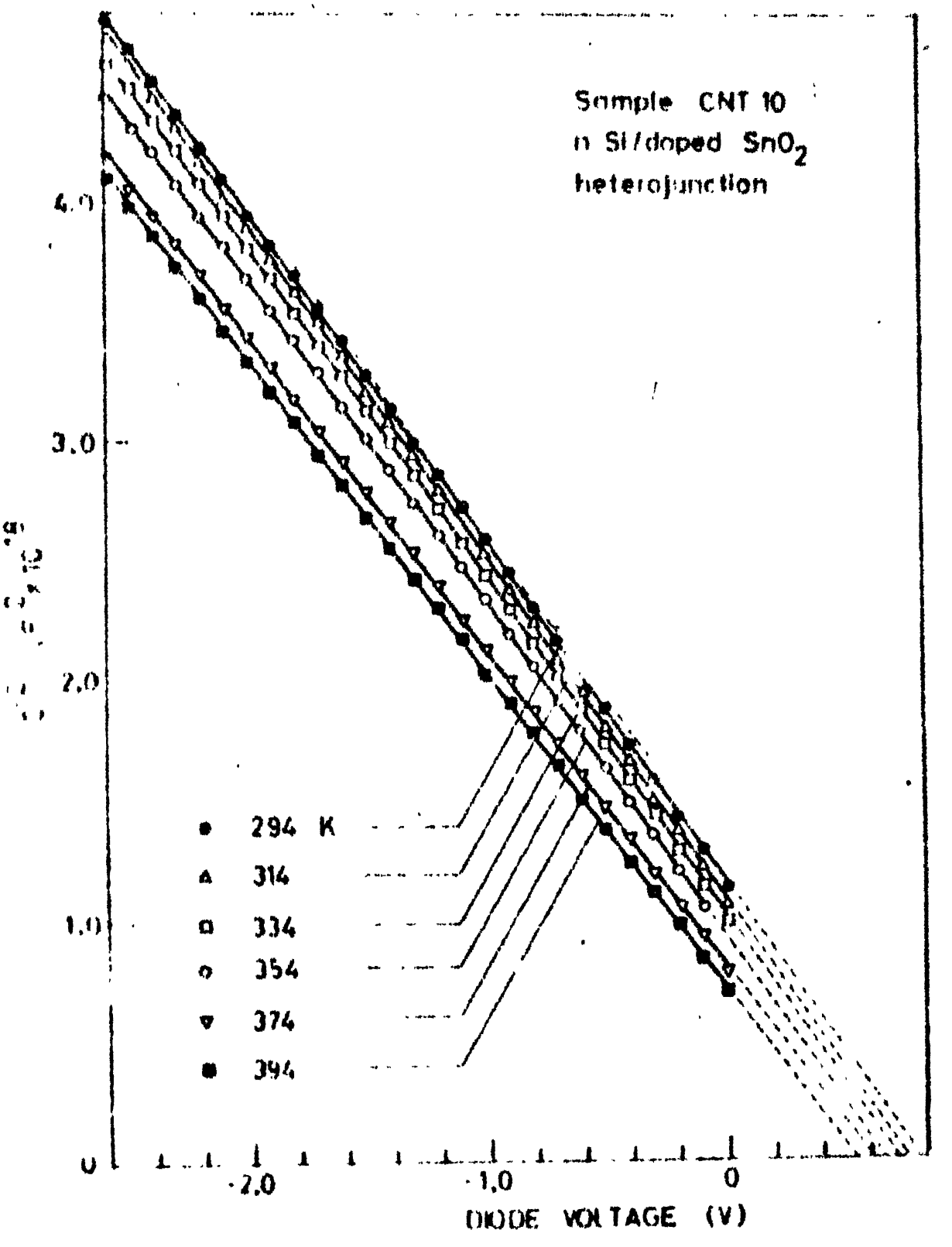


Figure 3.8 Measured 50 kHz C^{-2} vs V characteristics of a typical Sb-doped SiO_2-nSi heterojunction CNT 10 at device temperatures of 294, 314, 334, 354, 374 and 394°K

Table 3.2 : Experimental data of sample CNT 10 (Sb doped SnO_2-nSi heterojunction) obtained from measured I-V and C^{-2}-V characteristics

T (^oK)	n	nT (^oK)	J_o (A/cm^2)	ϕ_b^{eqv} (V)	N_D ($10^{15} cm^{-3}$) N_D^1	N_D^2	ϕ_n (V)	Ψ_i^o (V)	$\Psi_i^o+\phi_n$ (V)
294	2.31	679	4.3×10^{-7}	0.78	4.29	4.44	0.22	0.86	1.08
314	2.14	672	8.1×10^{-7}	0.82	4.29	4.44	0.24	0.81	1.01
334	1.97	658	1.7×10^{-6}	0.85	4.29	4.51	0.26	0.75	1.01
354	1.86	658	3.6×10^{-6}	0.88	4.29	4.58	0.27	0.67	0.94
374	1.73	656	6.8×10^{-6}	0.93	4.65		0.29	0.65	0.94
394	1.67	658	1.9×10^{-5}	0.94	4.65		0.31	0.57	0.88

the intermediate voltage regime. However, the characteristics of Figure 3.7 differ significantly in many respects from those of device CNT 15 in Figure 3.3. Most clearly visible is the feature that the slope of ln I vs V in Figure 3.7 is more or less invariant of the diode temperature. In other words, n decreases strongly with temperature so that the product n.T remains more or less a constant, cf. Table 3.2. In contrast, the slope of ln I_D vs V is Figure 3.3 decreases with increasing temperature such that n more or less remains constant, cf. Table 3.1. The value of n at T = 294^{o}K as 1.65 indicates the dominant mechanism in case of sample CNT 15 as recombination-generation. For diode CNT 10, the value of n is still higher at room temperature, i.e., n = 2.31. Further, the characteristics of sample CNT 15 in Figure 3.3 are more temperature sensitive than those of sample CNT 10 in Figure 3.7 and the reverse characteristics of sample CNT 15 are more voltage-sensitive than those of sample CNT 10. Lastly, in case of sample CNT 10, as Figures 3.5 and 3.6 indicate, ln J_o is a linear function of T instead of T^{-1} as in case of CNT 15.

The above features of sample CNT 10 indicate that an activated process such as thermionic emission, minority carrier injection, or recombination-generation is not involved in carrier transport in this device, but the most likely mechanism appears to be trap-assisted tunneling (multistep tunneling). It is interesting to note that both the

mechanisms of multistep tunneling and recombination-generation require the presence of traps in the space charge layer. Recombination-generation, however, indicates presence of single level traps while multistep tunneling requires multilevels of traps distributed in the space charge region. A large density of traps (comparable to donor density), if present, is expected to reflect itself in the reverse C^{-2} vs V characteristics of the device, specially at low frequencies and at high temperatures. Figures 3.4, 3.8 and Tables 3.1, 3.2 show that, like in the case of I vs V characteristics, the C^{-2} vs V characteristics of sample CNT 10 also deviate significantly from those of sample CNT 15. Worth noting are the following features :

(i) The C^{-2} vs V characteristics of sample CNT 15 can be represented by one straight line. But, those of sample CNT 10 have to be represented by two straight lines at temperatures of 294, 314, 334 and 354 ^{o}K, while the same at 374 and 394 ^{o}K can be represented by one straight line. Where the characteristics have two slopes, two values of doping density, N_D^1 and N_D^2, have been given in Table 3.2, N_D^1 being the density at smaller values of the reverse bias. It may be noted that in the temperature range of 294 -354 ^{o}K, N_D^1 is same, while N_D^2 keeps increasing. N_D^1 therefore corresponds to the donor density while N_D^2 has contribution from deep level traps also.

(ii) The decrease in the value of Ψ_i^o with increasing temperature is much larger in case of sample CNT 10 than in case of sample CNT 15, i.e., $\delta\Psi_i^o$ is - 0.29V in the temperature range of 294 - 394°K in case of sample CNT 10, while for CNT 15, $\delta\Psi_i^o$ is -0.14 V in the temperature range of 294 - 374°K. The corresponding change in the Fermi level, $\delta\phi_n$, in case of sample CNT 10 is only 0.09 V, so only a minor part of the decrease in Ψ_i^o can be explained by $\delta\varphi_n$. It therefore appears that V_{ox}^o in case of CNT 10, cf. Equation (3.3), increased by about 0.20 V over the above temperature range, compared to about 0.08 V for CNT 15, indicating a higher change in space charge density, δQ_{sc}, and/or there interface charge density, δQ_{ic}, with rise in temperature, for antimony doped SnO_2-Si heterojunction, compared to undoped SnO_2-Si heterojunction.

(iii) It appears from Tables 3.1 and 3.2, that the room temperature (294°K) heterojunction barrier height, $\Psi_i^o+\phi_n$, obtained from the C^{-2} vs V characteristics is higher for CNT 10 than that for CNT 15 by about 0.11 V. However, the zero-bias current density intercept J_o is higher for CNT 10 than for CNT 15. This is another indication that the mechanism of carrier transport is likely to be different in the two devices.

3.4.3 Response of Deep Level Traps

The role of deep level traps has been discussed in Section 3.2.3. Figures 3.4,3.8 and Tables 3.1,3.2 indicate the presence of a considerably large number of traps in the silicon space charge layer of sample CNT 10 than in the same of sample CNT 15. To confirm this indication, the reverse C^{-2} vs V characteristics of samples CNT 10 and CNT 15 were measured at lower frequencies of 1 kHz and 400 Hz.

Figure 3.9 contains the measured lower frequency reverse C^{-2} vs V characteristics of sample CNT 10. For comparison, the 50 kHz C^{-2} vs V characteristic measured at 294°K has also been included. This figure illustrates the differences between the characteristics, measured at 294°K, but at 50 kHz, 1 kHz and 400 Hz. In dark, 1 kHz characteristic is seen to deviate from the 50 kHz characteristic, while the 400 Hz characteristic deviated even further. The undulations observed in the 1 kHz and 400 Hz characteristics of sample CNT 10 measured at 294°K, could be related to what Roberts and Crowell [30] had predicted, on the basis of a theoretical analysis, to be due to rapid variation in the surface charge density with silicon band-bending, whenever the quasi-Fermi level intersects a trap level at the surface. The 1 kHz characteristics measured at 354 and 374°K do not exhibit any undulations, but, a single slope. Moreover, these two characteristics are very close to each other with the

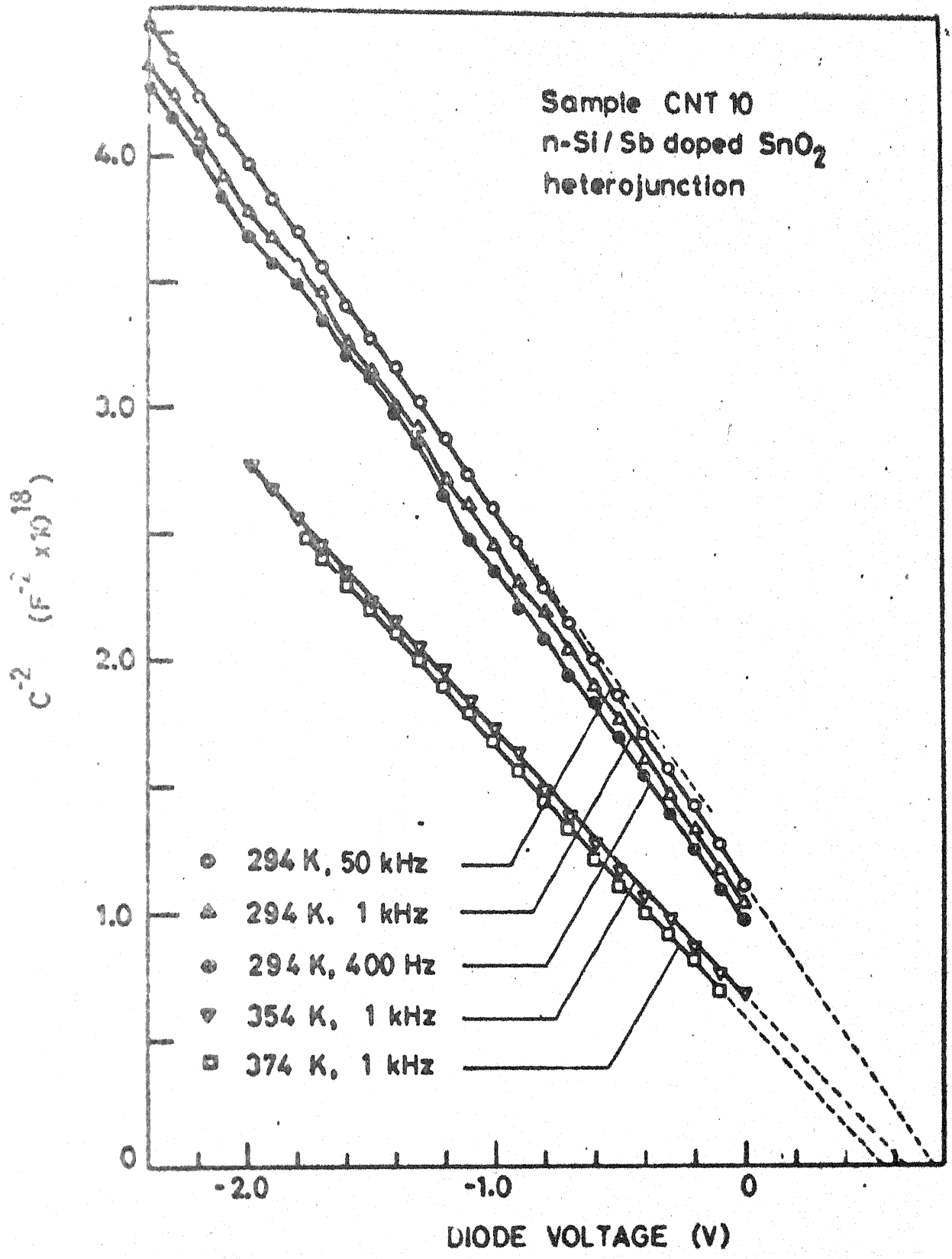


Figure 3.9 Reverse C^{-2} vs V characteristics of sample CNT 10 measured at 1 kHz and 400 Hz and at 294 and 354°K

same slope, and can be seen to deviate very strongly from the 50 kHz characteristic measured at 294°K. When compared to the 50 kHz characteristics of Figure 3.8, measured at 354 and 374°K respectively, it appears that these characteristics have considerably smaller slopes but about the same intercepts, c.f. Table 3.3.

The above features of the low frequency reverse C^{-2} vs V characteristics of sample CNT 10 and existance of two slopes in high frequency C^{-2} vs V characteristics at 294°K, confirm the presence of a large density of traps in the surface region of silicon. The characteristics of Figures 3.8, 3.9 also indicate that the response of the traps to the ac signal increases with decreasing modulation frequency and that deep multilevel traps are present, some of whose equilibrium frequencies may be very low. The C^{-2} vs V characteristics of sample CNT 15 measured at 1 kHz and 400 Hz and at 294 and 354°K, on the other hand, were observed not to deviate appreciably from those measured at 10 kHz indicating lower density of deep level traps compared to those expected in case of sample CNT 10.

It is important to state that, for both the samples CNT 15 and CNT 10, the temperature-bias stressing, in the temperature range for which the I_D vs V and C^{-2} vs V characteristics have been presented above, did not bring about any detectable physical change in the heterojunctions. To ensure

Table 3.3 : Experimental data obtained on device CNT 10 from C^{-2} [V,f] characteristics

T	N_D (10^{15} cm^{-3})			Ψ_i^o (V)	
	50 kHz		1 kHz	50 kHz	1 kHz
(^oK)	N_D^1	N_D^2	N_D		
354	4.29	4.58	5.77	0.67	0.67
374	4.65		5.77	0.65	0.63

this, after the measurements were completed at the highest temperature, the room temperature measurements were always completely repeated, besides partial checks at other temperatures.

It is not clear from the results obtained so far what the physical or chemical nature of the traps could be. From the fact, that a much larger density of traps are present in case of heterojunctions with doped tin oxide layers, one may be led to believe that at least some of the trap levels are related to antimony. However, if present in silicon in the elemental form and if occupying a substitutional site, antimoney will create a shallow level. Whatever be the exact chemical/physical origin of the various trap levels, it appears that at least some trap levels may be the consequence of extrinsic chemical impurities diffusing into the silicon surface region through the tin oxide layer during chemical vapor deposition. A fact which seems to have a bearing on this aspect is that during deposition of antimoney-doped tin oxide layers, a much larger amount of by-products were observed than in case of undoped tin oxide layer deposition. If a majority of traps are related to the by-products, then, the above fact could explain the presence of a much larger density of traps in case of heterojunctions with doped tin oxide layers.

3.4.4 Carrier Transport

The following trend seems to emerge regarding carrier transport across the transparent conductor-semiconductor heterojunction on the basis of results obtained in the present investigation and information available in literature [3-8,14, 20]. At lower temperatures, irrespective of the magnitude of the surface barrier height, the mechanism of field emission (direct tunneling) or thermionic field emission (thermionic tunneling) across the barrier can be expected to dominate carrier transport. At room temperature or higher, if the barrier height is not large, i.e., it is considerably lower than the silicon bandgap, thermionic emission can be expected to dominate carrier transport. On the other hand, if the barrier height is large and the trap density is low enough, then minority carrier injection can be expected to dominate carrier transport. However, if the barrier height is large and the trap density in space charge layer is moderate, then recombination-generation is likely to dominate, while in case of large density of traps, i.e., of the order of dopant density, multistep tunneling (trap assisted tunneling) may dominate.

Kato et al [6] are amongst early investigators of SnO_2/n-Si heterojunctions. They deposited tin oxide layers by spray hydrolysis at 300°C. They concluded thermionic emission as the dominant transport mechanism on the basis of activation plot resulting in medium barrier height of about 0.69 eV.

However, the diode quality factor, n, was 1.68 at 298°K whose value increased with temperature. It appears that apart from from thermionic emission, some other transport mechanism, like recombination-generation, may also have contributed to carrier transport. Such superposition of the current components has been reported on MOS diodes also [17].

Nagatomo et al [7] also used spray hydrolysis for fabrication of SnO_2/n-Si heterojunctions ,but at a deposition temperature of 600°C. Their measurements indicated a barrier height of about 0.77 eV at 300°K. The diode quality factor,n, at room temperature was 1.9. Over a certain temperature range, the slope of ln I vs V characteristics, i.e., the product n.T, was found to be independent of temperature. On the basis of these informations, they concluded that the dominant current components were due to recombination-generation and due to tunneling via interface states. They attributed the latter to lattice mismatch and impurities. Nagatomo et al also found the 10 kHz C^{-2} vs V characteristics to exhibit varying slopes and the voltage intercepts decreased with temperature by about 0.50 V over a temperature range of 199°K, a change too large to be explained by $\delta \phi_n$. Based on our results and discussion on sample CNT 10, it appears that the dominant transport mechanism in case of samples prepared by Nagatomo et al might have been multistep tunneling. Information on variation of ln J^o vs T^{-1} and T could have helped in this matter.

Feng et al [5] fabricated SnO_2/n-Si heterojunctions by electron beam evaporation of tin oxide followed by post-deposition annealing in air at 300°C. From reverse C^{-2} vs V characteristics, they obtained a large barrier height of about 0.87 V and their ln J vs V characteristics exhibited temperature-independent slope, i.e., n.T. was constant, in the temperature range of 274-357°K. They also obtained a very high value of diode quality factor, n, around 3.4. These facts suggest that the traps generated during electron beam deposition may have resulted in some trap assisted mechanism like multistep tunneling as the dominant transport mechanism, though this aspect was not investigated by them. They however seem to have arrived at a wrong conclusion that thermionic emission was the dominant current transport mechanism.

Ashok et al [3] fabricated In_2O_3/n-Si heterojunctions by spray hydrolysis of indium oxide at 400°C. They obtained a barrier height of 0.95 eV from the reverse C^{-2} vs V characteristics. The ln J vs V characteristics showed a temperature independent slope implying product n.T. to be constant. The ln J_o vs T plot was found to be linear. On the basis of these facts, Ashok et al concluded the dominant transport mechanism in their devices to be multistep tunneling.

Kar et al [34] compared the characteristics of an MOS diode fabricated on Wacker polycrystalline silicon with

In_2O_3/n-Si heterojunctions. They found many similarities between the characteristics and concluded multistep tunneling as the dominant transport mechanism in both cases on the basis of temperature-independent slope of the ln J-V plot, a weak dependence of diode current on temperature, a linear relation between ln J_o and T and a large decrease in Ψ_i^o with T than what can be accounted for by the corresponding change in ϕ_n or ϕ_p. A detailed investigation of carrier transport mechanism in MOS diodes on single crystal and polycrystalline silicon, by Kar et al [25] revealed that thermionic emission or minority carrier injection played the dominant role in carrier transport in case of the devices fabricated on single crystal silicon, while the devices on polysilicon showed either multi-step tunning or a combination of thermionic emission/minority carrier injection and multistep tunneling, depending on the type and density of imperfections/grain boundaries in poly-silicon.

Chang and Sites [8] fabricated In_2O_3/p-Si heterojunctions by ion beam deposition of indium oxide. On the basis of tem-perature-independent slope in ln J_o vs V curve, i.e. constant n.T, and linear dependence of ln J_o on T, they concluded the carrier transport to be dominated by trap-assisted tunneling (multistep tunneling). Further, their measured high frequency C^{-2} vs V characteristics exhibited slopes varying with reverse

voltage and also with temperature. The voltage intercept decreased with temperature by about 0.49V in the range of 200-400^{o}K which cannot be accounted for by the corresponding change in ϕ_p.

Ghosh et al [4] prepared SnO_2-nSi and In_2O_3-nSi heterojunctions using spray hydrolysis at 400^{o}C. The ln J vs V characteristics of their devices showed two slopes giving diode ideality factor $n_1 > 2$ at low and moderate forward voltages and $n_2 \sim 1$ at high forward voltages (greater than 0.7 V). The reverse saturation current J_o^1 corresponding to n_1 in low bias region was of the order of $1x10^{-6}$ A/cm^2 while J_o^2 corresponding to n_2 in high bias region was of the order of $1x10^{-11}$ A/cm^2. They have attributed the current at low bias region due to thermionic emission since $J_o^1 = A^* T^2 \exp(-\frac{q\phi_b}{kT})$, assuming $\phi_b \sim 0.8$ eV, gives reverse saturation current of the order of $1x10^{-6}$ A. Similarly they have attributed current at high forward bias region to minority carrier injection since $J_o^2 = p_n\, q\, D_p/L_p$ can justify the order of magnitude of current obtained ($\sim 10^{-11}$ A/cm^2). In the absence of detailed I-V and C-V analysis at different temperatures, they seem to have arrived at doubtful conclusions. The current at high bias may have been due to thermionic emission or minority carrier injection. However, large value of n_1 suggests a different transport mechanism at low bias. This could have been due to tunneling or recombination process.

The thermal and optical degradation of these devices has been studied by Maruska et al [9]. It has been reported that upon extended periods of exposure of these cells to UV light, the open circuit voltage degraded by about 5% while the short-circuit current and fill factor remained same. This could be reversed with the help of low temperature annealing ($100 < T < 200^{\circ}C$). The dark J vs V characteristics have been reported to change due to this optical degradation such that J_o^1 increased initially and then saturated while n_1 remains same. V_{oc} accordingly decreased and then saturated. The optical degradation is attributed to photo emission of electrons from Si to SiO_2 conduction band which are trapped leaving charge redistribution at Si-SiO_2 interface. The change in J_o^1 due to UV exposure, which causes radiation damage, introduces traps in depletion region and its reversibility due to annealing also indicates that the current at low bias may be due to recombination and tunneling processes, instead of thermionic emission as concluded by them. They have also found that if the devices are heated to more than $300^{\circ}C$, irreversible changes take place in dark I vs V characteristics. The slope of the I-V curve at low bias changes and n_1 changes from about 2.7 to unity. Once n_1 becomes close to unity, no further degradation takes place. The open circuit voltage reduces drastically and short-circuit current and fill factor also reduce. They have found this effect to be more predominant in SnO_2 devices

compared to In_2O_3 devices and have attributed this to chemical change in SiO_x layer in presence of SnO_2 arising from oxidation of SiO_x to form SiO_2 and reducing SnO_2. If this is true then the observed degradation can be explained in terms of changing of the structure with insulating interfacial layer to one that has a conducting interfacial layer (due to presence of Sn^+ ion) making it similar to Schottky barrier device.

Werthen et al [31] prepared Sn doped In_2O_3-pCdTe heterojunction solar cells formed by e-beam evaporation with efficiency of 10.5%. In_2O_3 layer thus formed was initially opaque and became transparent after heat treatment in air. ln J vs V of these devices showed a straight line and n was generally between 1.5 to 2.0. As deposited device showed $n \sim 2.0$ and $J_o \sim 10^{-8}$ A/cm^2, while after the heat treatment n reduced to 1.5 and J_o increased to 10^{-6} A/cm^2. The V_{oc} was found to be reduced due to heat treatment. $1/C^2$ vs V measurements revealed the barrier height as 1.0 eV for opaque film and 0.7 eV for transparent film. The lowering in barrier height is responsible for increase in J_o. On a typical device with n = 1.3, J vs V characteristics were measured as a function of temperature. Above 293°K n remained constant with temperature and they have attributed this to thermally activated recombination process. The plot of ln J_o vs 1/T gave an activation energy of 0.76 eV which is comparable with the value obtained from $1/C^2$ vs V plot. Below 293°K the

activation energy plot deviated from straight line and the current also became relatively insensitive to temperature variation. They have attributed this to tunneling current component. Upon studying the change with doping density, they found that n increases as doping density is reduced. They have attributed this to a change from thermally activated interfacial recombination process to bulk recombination process in case of lower doping density.

As mentioned earlier Riben et al [21,22] fabricated nGe-p GaAs heterojunctions where dominant mechanism was found to be multistep tunneling. Donnelly et al [23] fabricated pGe-nSi and pGe-nGaAs heterojunctions which showed multistep tunneling above a certain temperature and below this temperature the current was governed by thermally activated process. This they have explained in terms of thermally activated recombination process. In this process the majority carriers cross the barrier due to sufficient kinetic energy but get recombined at the interface states due to large density of states. This process will result in the I-V behaviour similar to thermionic emission but the current will also depend on density of interface states. Werthen et al [31] have attributed current in their devices due to this process.

Krupanidhi et al [32] studied J vs V and C vs V characteristics of As_2Te_3-Si heterojunctions. They found that at low bias, the current changed rapidly but exponentially with

voltage but in high bias region the current changed relatively slowly though still exponentially. Thus the value of n_1 at low bias was small while that of n_2 at high bias was large. Upon temperature variation, the slope of ln I vs V plot in low bias region was found to increase such that n_1 decreased with temperature, but the slope in high bias region remained constant. Also ln J_o^1 vs 1/T was found to be a straight line in low bias region while ln J_o^2 vs T gave a straight line in high bias region. They have attributed the current in low bias region to thermally activated process and the activation energy from ln J_o vs 1/T plot was found to be 0.185 eV. The current in high bias region has been attributed to multistep tunneling process.

Recent investigations by Zemel et al [33] on carrier transport in p.GaAs-n$Ga_xAl_{1-x}As$ heterojunctions seem to have an interesting bearing on the topic of present work, though a different semiconductor material and nature of junction is involved. Liquid phase epitaxy was used for fabrication of these heterojunctions. At low and moderate forward bias, they found, in most of the devices, n.T. to be temperature-independent and ln J_o vs T to be linear. On the basis of these they identified the dominant transport process to be multistep tunneling and suggested that the traps were introduced during processing. It is equally interesting to note that in case of a small number of devices, their data on the diode quality

factor n and the activation plots indicated the transport mechanism to be dominated by recombination at low and moderate bias. This probably may be due to lesser number of traps in these samples.

Nielsen [17] has examined current transport mechanism in Al-SiO_x-pSi devices with oxide thickness around 20Å and silicon doping density in the range of 10^{14}-10^{16} cm^{-3}. In J vs V characteristics showed two straight lines. At lower bias $n_1 > 1$ while at higher bias $n_2 \sim 1$. As temperature is increased, n_1 reduced while n_2 remained constant. The current at high bias has been attributed to minority carrier injection which has been differentiated from thermionic emission from temperature variation of reverse saturation current. They have found that as the doping was increased, the current in low bias range increased while that at high bias reduced. On the basis of increase in diode current with doping density which can be explained by Equation (3.16), they have concluded multistep tunneling to be the dominant mechanism at low bias. It is interesting to note that $n_1.T$ in their case was not constant with temperature. Moreover, multistep tunneling in case of single crystal silicon MOS devices is unlikely mechanism [25]. It is therefore doubtful if their devices showed multistep tunneling in low bias region. Probably the low bias region was dominated by recombination current which increase with doping density due to reduction in minority carrier lifetime.

Table 3.4 summarizes the experimental data obtained by various investigators discussed above as well as during present study, which reflect on the carrier transport and presence of traps in the heterojunction region. The previous discussion and an inspection of Table 3.4 reveals that in majority of SnO_2-Si and In_2O_3-Si heterojunctions with a high barrier, trap-assisted tunneling is likely to be the dominant mechanism of carrier transport, otherwise recombination-generation may prevail. The crucial factor in this context is the generation of traps in the active heterojunction region during processing. Presence of traps can perhaps be reduced by proper selection of processing steps and techniques. If density of traps can be reduced below a critical level, minority carrier injection may finally be the dominant transport process with attendant increase in the slope of ln I vs V curve, i.e., n will approach unity. As Table 3.4 indicates, most of the silicon-transparent conductor heterojunctions show high open-circuit voltage due to a high value of surface barrier attained. However, the fill factor is generally poor due to high value of diode ideality factor, n, which seems to be typical of trap-assisted tunneling. The trap assisted tunneling process, as discussed in Section 3.2 is given by the expression (3.17)

$$J_{mt} = J_{mto} \exp(AV) \exp(BT)$$

Table 3.4(a) : Experimental data obtained by various investigators on parameters related to carrier transport in transparent conductor - semiconductor heterojunctions

Reference	Heterojunction	n[T]	n at 300°K	J_o[T]	A (V^{-1})	B (K^{-1})	Dominant transpo mechanism identi fied by author
1	2	3	4	5	6	7	8
Ashok et al [3]	In_2O_3-nSi spray hydro- lysis at 400°C	n.T constant in the range 301-351°K	1.68	ln J_o li- near fun- ction of T	23.0	0.050	multistep tunneling
Ghosh et al [4]	SnO_2-nSi spray hydro- lysis at 400°C	not investi- gated	>2.0 at low bias ~ 1.0 at high bias	not inves- tigated	-	-	thermionic emissi at low bias minority carrier injection at high bias
Feng et al [5]	SnO_2-nSi e-beam evapora- tion and annealing at 400°C	n.T constant in the range 274-357°K	3.44	not plotted	not given	not given	thermionic emission
Kato et al [6]	SnO_2-nSi spray hydro- lysis at 300°C	n increased with T in the range 198- 348°K	1.68	ln J_o linear function of 1/T	-	-	thermionic emission

contd ...

1	2	3	4	5	6	7	8
Nagatomo et al [7]	SnO_2-nSi spray hydrolysis at 600°C	n.T constant	1.90	not plotted	not given	not given	generation-recombination and tunneling
Chang et al [8]	In_2O_3-pSi ion beam sputtering	n.T constant in the range 200-410°K	1.60	ln J_o linear function of T	23	0.064	multistep tunneling
Werthen et al [31]	In_2O_3-pCdTe e-beam evaporation	n constant above 293°K	1.30	ln J_o linear function of 1/T	-	-	thermally activated recombination process
Present investigation[26]	Undoped SnO_2-nSi by CVD at 300°K	n constant in the range of 294-374	1.65	ln J_o linear function of 1/T	-	-	recombination-generation
	Sb doped SnO_2-nSi by CVD at 300°K	n.T constant in the range 294-394°K	2.31	ln J_o linear function of T	17.0	0.035	multistep tunneling

Table 3.4(b) : Experimental data obtained by various investigators on parameters related to traps

Reference	$\phi_i + \phi_n$ at 300°K (high f) (V)	$\phi_i[T]$ (V)	$dc^{-2}/dV[T,V]$	$C^{-2}[V,f,T]$	V_{oc}	F
1	2	3	4	5	6	7
Ashok et al [3]	0.95	not investigated	not investigated	not investigated	0.49	0.63
Ghosh et al [4]	not investigated	not investigated	not investigated	not investigated	0.52	0.55
Feng et al [5]	0.87	not investigated	not investigated	not investigated	0.53	0.65
Kato et al [6]	0.69	not investigated	not investigated	not investigated	not given	not given
Nagatomo et al [7]	0.77	decreased by 0.50V in the range 110-299°K	slope varied with reverse bias	not investigated	0.32	0.51
Chang et al [8]	1.02	decreased by 0.49V in the ranges 200-400°K	slope varied with reverse bias and with T	not investigated	0.51	0.72

contd ...

1	2	3	4	5	6	7
Werthen et al [31]	0.70	not investigated	not investigated	not investigated	-	-
Present investigation [26]	0.97	decreased by 0.14 V in the range 294-374°K	slope T and V invariant	no change in characteristics at low f	-	-
	1.08	decreased by 0.29V in the range 294-394°K	slope varied with V and T	at low f undulations in characteristics at 300°K, and smaller slope at higher T	-	-

It is apparent that A = q/nkT and for n = 1 its value should be 39 V^{-1} at room temperature. Since A is found to be much smaller, as Table 3.4(a) shows, where trap assisted tunneling dominates, fill factor can be expected to be lower due to larger value of n. Therefore, if this current component can be reduced by choice of suitable processing, minority carrier injection may became the dominant transport mechanism resulting in increase in fill factor. An inspection of Figures 3.7, 3.8 shows that for sample CNT 10, the voltage shift in the ln J vs V characteristics for a constant I is 0.25V while the decrease in Ψ_i^o is 0.29V between 294 and 394°K. This suggests that the temperature dependence of I_{mt} reflects the change in Ψ_i^o with temperature. Such a correlation was found also by Chang and Sites [8].

3.5 CONCLUSIONS

In case of undoped tin oxide-Si heterojunctions, typical ln J vs V characteristics exhibited a nearly temperature-independent n, and ln J_o was a linear function of T^{-1} resulting in an activation energy of about 0.58 eV, while the barrier height obtained from reverse C^{-2} vs V plot was 0.97 eV at room temperature. These data indicated the dominant transport mechanism to be recombination-generation. In case of antimony doped tin oxide, ln J vs V characteristics exhibited a temperature-independent slope, and ln J_o was found to be a linear function of T, on the basis of which the dominant transport

process was identified as trap-assisted tunneling. In case of the undoped tin oxide, the higher frequency C^{-2} vs V characteristics exhibited a single temperature-independent slope, and the voltage intercept decreased by 0.14 V with increasing temperature in the range 294-374°K. Further, the lower frequency C^{-2} (V,T) characteristics did not deviate appreciably from those at higher frequency. On the other hand, in case of antimony-doped tin oxide, the higher frequency C^{-2} vs V characteristics exhibited voltage dependent and temperature dependent slopes, and the voltage intercept decreased strongly by 0.29 V, with increasing temperature in the range of 294-394°K. Moreover, the lower frequency C^{-2} vs V characteristics deviated strongly from the higher frequency characteristics, and exhibited undulations at 294°K, but a single slope free from undulations above 354°K. The experimental C^{-2} (V,T,f) data indicated the presence of a large density of multilevel traps in the active heterojunction region of Sb-doped SnO_2/n-Si devices. The results also indicated that the temperature dependence of the multistep tunneling current is a consequence of the decrease in the zero-bias silicon band-bending with T. The dominance of multistep tunneling in SnO_2/n-Si heterojunction solar cells, with attendant high value of n leads to a lower fill factor F, although V_{oc} is generally high owing to a large barrier height. Reduction in trap density

References

1. T. Feng, D.J. Eustace, and A.K. Ghosh, Proc. 16th IEEE Photovoltaic Specialists Conf., (1982).

2. E. Saucedo and J. Mimila-Arroya, Proc. 14th IEEE Photovoltaic Specialists Conf., 1370 (1980).

3. S. Ashok, P.P. Sharma, and S.J. Fonash, IEEE Trans. Electron Devices ED-27, 725 (1980).

4. A.K. Ghosh, C. Fishman and T. Feng, J. Appl. Phys. 49, 3490 (1978).

5. T. Feng, C. Fishman and A.K. Ghosh, Proc.13th IEEE Photovoltaic Specialists Conf., 519 (1978).

6. H. Kato, J. Fujimoto, T. Kanda, A. Yoshida, and T. Arizumi, Phys. Stat. Sol. 32, 255 (1975).

7. T. Nagatomo, M. Endo and O. Omoto, Jap. J. Appl. Phys. 18, 1103 (1979).

8. M.S. Chang and J.R. Sites, J. Appl. Phys. 49, 4833 (1978)

9. H.P. Maruska, A.K. Ghosh, D.J. Eustace and T. Feng, J. Appl. Phys. 54, 2489 (1983).

10. J. Schewchun, J. Dubow, C.W. Wilmen, R. Singh, D. Burk and J.F. Wager, J. Appl. Phys. 50, 2832 (1979).

11. R. Singh, M.A. Green, and K. Rajkanan, Solar Cells 3, 95 (1981).

12. P.P. Sharma, T.C. Anthony, S. Ashok, S.J. Fonash and L.L. Tongson, Jpn.J. Appl.Phys.(Suppl.1)19,551 (1980).

13. S. Kar, S. Varma, P. Saraswat and S. Ashok, J.Appl. Phys. 53, 7039 (1982).

14. E.H. Rhoderick, 'Metal-Semiconductor Contacts, (Clarendon, Oxford, 1978).

15. S. Kar and W.E. Dahlke, Solid State Electron. 15, 869 (1972).

16. S. Kar and W.E. Dahlke, Solid State Electron 15, 221 (1972).

17. O.M. Nielson, J. Appl. Phys. 54, 5880 (1983).

18. S.M. Sze, 'Physics of Semiconductor Devices', (John Wiley and Sons, Inc. New York, 1969).

19. F.A. Padovani and R. Stratton, Solid-State Electron. 9, 695 (1966).

20. A.N. Saxena, Surface Science 13, 151 (1969).

21. A.R. Ribben and D.L. Feucht, Solid State Electron 9, 1055 (1966).

22. A.R. Ribben and D.L . Feucht, Int. J.Electron. 20, 583 (1966).

23. J.P. Donnely and A.G. Milnes, Proc. IEE 113, 1468(1966).

24. S. Kar, S. Ashok, and S.J. Fonash, J. Appl. Phys. 51, 3417 (1980).

25. S. Kar, K.M. Panchal, S. Bhattacharya and S. Varma, IEEE Trans. Electron Devices, ED-29, 1839 (1982).

26. S. Varma, K.V. Rao and S. Kar, J.Appl. Phys. XX,XXXX (1984).

27. O.M. Nielsen, IEE Proc. 1, Solid State Electron Devices 127, 301 (1980).

28. S. Kar, Appl. Phys. Letters 25, 587 (1974).

29. S. Wang, 'Solid State Electronics', (McGraw Hill, New York, 1966), p.210.

30. G.I. Roberts and C.R. Crowell, J.Appl.Phys. 41, 1767 (1970).

31. J.G. Werthen, A. L. Fahrenbruch, R.H. Bube and J.C. Zesch, J.Appl.Phys. 54, 2750 (1983).

32. S.B. Krupanidhi, R.K. Srivastava, K. Srinivas, D.K. Bhattacharya and A. Mansingh, J.Appl. Phys. 54, 1383 (1983).

33. A. Zemel, H.W. Willemson, K.D. Andersen, and F.R. Shepherd, J.Appl. Phys. 54, 1981 (1983).

CHAPTER 4

INTERFACE INVESTIGATION USING TRANSPARENT CONDUCTOR-OXIDE-SILICON STRUCTURES UNDER ILLUMINATION

4.1 INTRODUCTION

The $Si-SiO_2$ interface posses electronic defects such as interface states, fixed surface charges, ionized traps, and mobile ions [1,2]. The interface states are the energy levels within the forbidden energy gap at the insulator-semiconductor interface which can exchange charges with the semiconductor bands easily. Interface state investigations have revealed a continuous distribution of interface states throughout the band gap which are generally attributed to dangling silicon bands at the interface. The density of these states and their distribution in the band gap depend on silicon orientation, oxidation conditions, post oxidation heat treatments, and various post oxidation processing steps involving energetic particles [2]. The interface states cause the capacitance-voltage characteristics of metal (or transparent gate) - oxide-silicon structures to deviate considerably from the ideal characteristics (assuming no interface states), and they govern the performance of all the surface barrier devices to a large extent. Fixed surface charges do not participate in change exchange but cause a parallel shift of the capacitance-voltage

characteristic along the voltage axis. Ionized traps also cause a voltage shift of the MOS capacitance-voltage curve, while mobile ions cause drift of these characteristics with time [1,2]. The mobile ions are generally alkali ions which can be minimized by taking suitable care during processing. Surface defects (states and traps), their origin, effect of various processing steps used in fabrication of modern electronic devices on these defects, and reduction of surface defects by suitable heat treatment steps, are problems of considerable interest, since most of the modern electronic devices employ $Si-SiO_2$ structure.

Various physical processes like sputtering, e-beam deposition, ion milling, ion implantation, electron beam lithography, etc. involving energetic particles are commonly used in modern electronic device processing. These energetic particles are known to cause radiation damage, and their effect on interface state density distribution needs to be studied in detail, so as to improve the performance of these devices. The interaction of radiation with thermally grown $Si-SiO_2$ interface results in creation of additional interface states and build up of fixed positive charges which can mostly be annealed out unless radiation energy is high [3,4]. The radiation energy is transferred to the Si-O network with liberation of electrons and holes. Many of these recombine, but most of electrons diffuse away due to greater mobility

leaving behind trapped holes near the interface. Thus positive fixed charge builds up at the interface resulting in shift in flat band voltage. The liberation of electron-hole pairs also causes surface states due to dangling bands. Physically, three different processes may contribute to the creation of interface states and build up of positive charges at the interface. These are atomic displacement, primary ionization and secondary ionization [3]. High energy particles, such as fast neutrons or massive ions, may physically knock away a network atom causing atomic displacement. This displaced atom, in turn, may knock away other network atoms in its path, until it looses all the kinetic energy. This results in a multitude of broken bonds giving rise to large density of interface states, and liberated electron-hole pairs cause build-up of trapped positive charges near the interface as explained above. The density of these trapped holes is greater near the interface and their position is influced by the field in the oxide during irradiation [3]. Ionizing radiations such as γ-rays, energetic electrons, very light ions, X-rays, and UV light, transfer energy to the Si-O network by highly exciting bonding electrons, breaking Si-O network, and creating electron-hole pairs. Again the broken bonds create interface states and density of trapped holes builds up near interface. This process is termed as primary ionization [3]. Secondary ionization results from the interaction of electrons created by

atomic displacement and primary ionization with defects in Si-O network, such as OH terminations or Si atoms near the interface [3]. This again results in creation of electron-hole pairs, increasing densities of interface states and surface charges. In addition to generation of interface states and fixed surface charges, irradiation by ions, electrons, energetic neutral atoms, photons etc. may also cause dielectric leakage in SiO_2 and build up of mobile charges in $Si-SiO_2$ system [4]. Build up of mobile changes may generally be observed in case of bombarding ions due to movement of previously immobile atoms in the oxide at room temperature [4].

The effect of radiation damage produced by various processes, used in modern electronic device fabrication, on interface properties, and annealing of these defects are being studied for past few years to determine the suitability of these processes and subsequent annealing steps [2-13]. Processes involving energetic electrons such as electron-beam deposition, electron-beam lithography, etc. cause increase in interface state density and fixed surface charge density due to ionization caused by energetic electrons as well as X-rays produced [2-9]. Accelerating potential of about 25 keV, generally used in electron beams, is too low to cause atomic displacement, but is believed to generate interface states, positive trapped charges and neutral traps by ionization process. The X-rays produced by electron beam also cause

similar damage [3]. Most of these defects can be annealed at about 450-550°C in forming gas or inert ambient [3,5-8], but effective removal of neutral traps is reported to require temperatures in the range of 700-900°C [3,8]. Interface investigations using admittance measurements have revealed a peak around 0.30 eV below conduction band having magnitude of about 10^{12} $cm^{-2}v^{-1}$, which increased and its position shifted towards conduction band edge with increase in electron dose [8,10]. DLTS measurements have revealed a peak around 0.08 eV below conduction band with a very low electron capture cross-section of 10^{-19} cm^2 [8]. In addition to damage at the interface, electron beam has been found to generate positively charged and neutral traps in SiO_2 which cause electron trapping. The positively charged traps are found to have capture cross-section of 10^{-13} cm^2 while that in case of neutral traps has been found to be 10^{-15} cm^2 [6]. The capture cross-sections associated with neutral as well as positively charged traps in SiO_2 showed field dependence [6]. Processes involving energetic ions like ion milling, reactive ion etching and ion implantation also produce interface states and traps. Ion implantation may cause interface damage due to all the three physical processes like atomic displacement, primary ionization, and secondary ionization, but reactive ion etching generally causes damage due to ionization processes [3,11]. Most of the positively charged traps and interface states can be annealed

out easily but removal of neutral traps is reported to require high temperature [3]. The effects occuring in plasma systems, encountered in plasma deposition or etching processes, are most difficult to understand due to variety of energetic particles present. Plasmas contain positive ions, negative ions, electrons, energetic neutral atoms, metastable atoms, X-rays, ultraviolet rays, etc. [4]. These can cause dielectric breakdown, interface states, traps, and mobile charges [4]. The effect of plasma on interface properties have been studied by some investigators [4,12-15]. The dielectric breakdown is not annealable, annealing at 500°C is found to remove most of interface state and fixed charge degradations, while removal of mobile ions is found to require annealing above 900°C [4,12]. Triode sputter etch cleaning of silicon prior to sputter deposition has been found to generate acceptor states in p-channel CMOS capacitor with midgap value of the order of 1×10^{10} cm^{-2} V^{-1} and a peak (10^{11}-10^{13} cm^{-2} V^{-1}) at 0.20 eV above flat band whose magnitude increased with duration of ething [12]. Sputter deposition of metal electrodes has been reported to result in a small peak ($1-7 \times 10^{10}$ cm^{-2} V^{-1}) below the flat band voltage due to initial exposure of the surface to ultraviolet radiation. Sputter etching of metal pattern by rf sputtering is reported to reveal a peak slightly above flat band whose magnitude depends on the power of sputtering [12]. All these defects are easily annealed. Magnetron

sputtering system has been reported to give rise to very little degradation at $Si-SiO_2$ interface under optimum conditions, which has been attributed to an equilibrium between creation and annealing of defects due to self heating of substrate [13].

Over the past two decades, the MOS structure has been used to great advantage for obtaining very reliable data on the interface state density distribution and other surface parameters from surface admittance measurements [2,9]. Various admittance techniques employed for interface investigations are given in texts [1,14]. They employ either high or low frequency capacitance measurements [15-18] or conductance measurements at various frequencies [19]. High frequency capacitance method proposed by Termen [15] is useful only if interface state density is large but uncertainity about the magnitude of the semiconductor depletion-layer capacitance make this method unreliable [1]. Low frequency capacitance method proposed by Berglund [16] gives more reliable interface state profile compared to high frequency method. In addition to these methods, the quasi-static capacitance method proposed by Kuhn [17] combines measurement of high frequency and low frequency C-V curves and eliminates the need for calculating space charge capacitance, which is required in low frequency method of Berglund [16]. However, measured high frequency capacitance, even at 1 MHz at times, does not correspond to ideal high frequency curve, which

should be due to only space charge capacitance. Hence, interface state density obtained by the quasi-static capacitance method may be lower than the actual density of states. These capacitance methods do not give correct interface state profile near the band edges. Temperature procedure proposed by Gray and Brown [18] gives interface state distribution in the region close to the band edges. The capacitance methods involve simple data analysis and give the sum total of all the states at a particular band energy, but do not give any information about capture cross-sections of these states, which can help in identifying the nature and origin of states. The conductance technique proposed by Nicollian and Goetzberger [19] gives very accurate and reliable results especially for low interface state densities ($\sim 10^{10}$ states/cm^2/ V) in majority carrier band gap half. In addition to giving interface state densities, the conductance procedure also gives majority carrier capture cross-section of states. It can give the break-up, if states with different capture cross-sections are present in the same region,and can provide interface state distribution of each group of states with different capture cross-sections. However, the analysis of conductance data is quite involved and was the major limitation of this method till now. Today powerful tools are available for admittance-voltage measurements. The HP 4192A LF impedance analyser which operates in the range of 5 Hz to 13 MHz, and can be

easily automated and interfaced with a desk top computer, greatly facilitates G-V measurements and related data processing in a very short time.

The surface admittance measurements, in almost all the cases, were carried out in the dark conditions. Su et al [20] recently suggested that in addition to reducing the thickness of oxide layer and using low carrier concentration substrates, use of low level illumination at a wavelength that creates electron-hole pairs, can be employed to extend the capabilities of capacitance and conductance techniques. Though they have carried out interface investigation in a metal-thin oxide (250 Å) - silicon structure using a combination of capacitance and conductance measurements under illumination [21], details of data analysis are not given. Determination of quasi-Fermi level separation becomes essential under illumination to assign proper band energy to the observed state densities. Results of Sher et al [21] do not mention about quasi-Fermi level separation and hence the interface state profile obtained by them may not be very reliable. Using the MOS structure with a semitransparent metal, Poon and Card [22,23] have recently shown that optical illumination lends the conductance technique access to the minority carrier band gap half and to interface state capture cross-sections for minority carriers. They have determined quasi-Fermi level separation, for a range of illumination levels, with the help of involved calculation of the

semiconductor space charge as a function of the surface potential for each illumination [23].

In dark, the interface states are expected to exchange charge with the majority carrier band. Information about interface states near the minority carrier band edge cannot be obtained by quasi-static technique in dark, especially if they have small capture cross-section for majority carriers, but these states can be accessed easily under illumination, since inversion layer response time greatly reduces under illumination. By suitably varying the illumination level, reliable interface state profile over most of the band gap can thus be obtained by surface admittance measurements. Conductance measurements under illumination yield electron capture cross-section (σ_e) of upper half band gap states, and hole capture cross-section (σ_h) of lower half bandgap states. These capture cross-sections may differ by orders of magnitude, and knowledge of both may help inidentifying the nature of states, e.g., acceptor states will have $\sigma_h >> \sigma_e$. Interface investigation in case of ultrathin oxides for VLSI applications can be carried out in dark by quasi-static technique only at high ramp rate due to large leakage current and device drift. A large number of states cannot respond to high ramp rates and information about them cannot be obtained. In such cases capacitance-voltage and conductance voltage measurements under illumination can be used to get interface state profile.

The transparent conductor-oxide-semiconductor (TCOS) structure closely resembles the metal-oxide-semiconductor (MOS) structure. If the transparent conductor is sufficiently conducting, as generally is the case, its energy bands may be assumed to be flat, as in metal. Consequently, energy bands will bend in the base semiconductor alone, and the TCOS structure reduces to a surface barrier device like MOS. It can, therefore, be used to investigate the semiconductor-insulator interface using the above mentioned surface admittance techniques. In fact, the TCOS structure may prove to be a superior tool for interface investigation then the MOS structure, especially if optical illumination is employed to extend the capabilities of surface admittance techniques. The TCOS structure offers the following advantages over the MOS structure. It is easier to deposit a transparent conductor, typically 2000 Å thick, than to deposit a semitransparent metal (less than 100 Å thick). The semitransparent metal film absorbs considerable amount of light, is chemically and structurally unstable, and often its durability is a problem during long measurements. None of these problems are encountered in case of indium or tin oxide. We have demonstrated the suitability of TCOS structures for $Si-SiO_2$ interface investigation under illumination, by the low frequency capacitance technique which is simpler compared to conductance technique [24]. We have also presented three simple and direct methods for experimentally determining quasi-Fermi level separation, from

measurement of either high or low frequency capacitance-voltage characteristics of a TCOS structure in dark and under illumination [25,26]. Though the capacitance and conductance techniques can be independently used in dark to get reliable data about interface states, we have shown that in case of measurements under illumination, both the capacitance and conductance data should be used together to get reliable information about interface states easily [26].

Transparent conductors have been used to fabricate highly efficient solid state imaging devices [27-32]. The performance of all these devices is governed by interface defects, and hence interface investigation becomes important. All the interface investigations in solid state imaging devices till now have been carried out in dark. Our investigations under illumination show existance of optically activated states whose magnitude changes and peak position shifts with illumination level [26]. Knowledge about interface state distribution under illumination, especially for opto-electronic devices, becomes important in the above context. Since transparent conductors can be deposited by variety of physical and chemical deposition processes, TCOS structures can be used for studying the effect of various process, parameters on interface defects. This can be helpful in improving the understanding of these processes and determining their suitability for modern electron device processing.

The aim of the present investigation was to demonstrate suitability of TCOS structure for interface investigation under illumination; to obtain interface state profile in TCOS structures prepared by spray deposition, chemical vapor deposition, and electron-beam deposition; and to study the effect of illumination level on the interface state density distribution in each case. The main aspect of this investigation was to establish a simple and reliable interface investigation technique employing capacitance and conductance measurements under illumination. Thermally oxidized SiO_2-Si system, without annealing, has been used for the interface state investigation. There are two reasons for using unannealed samples. Firstly, unannealed samples are reported to have higher interface state density and exhibit peaks in the profile. Such an interface becomes more useful if a technique for the investigation is to be developed, as was done in the present case. Secondly, unannealed samples will be a better tool to study various mechanisms involved in the process of deposition, which generate interface states. The nature and origin of these states can help in better understanding of the processes. It has been demonstrated that very useful additional information can be obtained by admittance data under illumination compared to that obtained in dark. Interface investigation has been carried out by the technique proposed, on TCOS structures prepared by above mentioned three

deposition processes. The effect of illumination level on the interface state profile has been studied in each case. To our knowledge, use of TCOS structure for investigation of the interface states by surface admittance measurements under illumination has not been reported so far.

4.2 EXPERIMENTAL DETAILS

Transparent conductor-oxide-silicon structures fabricated by spray deposition of Sn doped In_2O_3 films, chemical vapor deposition of undoped and Sb doped SnO_2 films, and electron-beam deposition of Sn doped In_2O_3 films were employed for $Si-SiO_2$ interface investigation using admittance measurements under illumination. The details of sample fabrication by different deposition techniques, and the electrical measurements carried out are given below. Sample fabrication was carried out in class 100 clean atmosphere .

4.2.1 Fabrication of Spray Deposited Sn Doped $In_2O_3-SiO_2-Si$ Structures

These samples were fabricated on n- and p-type single crystal silicon wafers, one side polished and other side lapped, with (111) surface orientation, and having resistivity of the order of 10 Ohm-cm. The wafers were initially degreased in warm trichloroethylene, warm acetone, and warm methanol. These were then rinsed in deionized water. After degreasing

and etching of intrinsic oxide, the wafers were loaded on a fused silica boat, and oxidation was carried out at 700°C in a resistance heated furnace having fused silica furnace tube, in dry oxygen ambient. The oxide thickness was kept in the range of 0-400 Å. Following oxidation, Sn doped In_2O_3 dots of approximately 1.0 mm diameter were deposited on the polished side of the wafer, by spray hydrolysis, using glass shadow masks. An alcoholic solution of $InCl_3$ and $SnCl_4 \cdot 5H_2O$, containing 2.5 wt% $SnCl_4$, was used as the source for spray deposition and the substrates were kept at 400°C. The spray deposited samples, without back metallization, were fabricated at Pennsylvania State University and details of spray deposition are reported elsewhere [33].

The polished surface of the wafers having In_2O_3 dots were masked with apiezon wax and the samples were etched in hydrofluoric acid to remove oxide layer from the back surface. Apiezon wax was subsequently removed in warm trichloroethylene and the samples were degreased again in warm solvents. Immediately, after back oxide removal, the samples were loaded in an oil free vacuum chamber and the back ohmic contacts were deposited by vacuum evaporation. Aluminium was used as the back ohmic contact metal on n-type silicon while gold was used for the same purpose on p-type silicon.

4.2.2 Fabrication of Chemical Vapor Deposited Undoped and Sb Doped SnO_2-SiO_2-Si Structures

These samples were fabricated on n-type epitaxial silicon wafers with (100) surface orientation and layer resistivity of 1.0 Ohm-cm. The wafers were degreased in warm trichloroethylene and warm acetone. They were then ultrasonically cleaned in acetone, degreased in warm methanol, rinsed in deionized water, etched in hydrofluoric acid, and finally rinsed in deionized water again. The deionized water used during wafer cleaning had a resistivity of 14-16 M Ohm-cm. After rinsing, the wafers were dried in dry filtered nitrogen gas at the mouth of oxidation furnace. Preoxidation was then carried out in a Thermco resistance heated furnace in dry oxygen at 1100°C for 30 minutes at atmospheric pressure. The preoxidized wafers were then etched in hydrofluoric acid, rinsed in deionized water, ultrasonically cleaned in acetone, etched again in hydrofluoric acid and finally rinsed in deionized wafer and then dried in dry nitrogen . Final oxidation was carried out immediately after etching and drying of preoxidized wafers in dry oxygen at atmospheric pressure. The preoxidation step was a part of wafer cleaning procedure which resulted in wafer surface free from silicon dust which was otherwise found on wafer surface after wafer scribing. Final oxidation was carried out at 1100°C for 15-30 minutes to

obtain oxide thickness in the range of 500 - 800 Å. No post oxidation annealing was carried out. Deposition of SnO_2 dots was done immediately after oxidation.

The chemical vapor deposition set up and details of deposition of undoped and Sb-doped SnO_2 films on oxidized silicon wafers are described in detail in Chapter 2. $SnCl_4.5H_2O$ was used as source for tin, deionized water was used as the oxidizing agent, while $SbCl_3$ was used as source for antimony in case of doped samples. The tin and antimony sources were kept at 93°C while deionized water was kept at 23°C. Chemical vapor deposition was carried out in a standard resistance heated furnace at a temperature of 300°C. Nitrogen was used as the carrier gas and the typical flow rates were 1250 cc/min through deionized water, 550 cc/min through molten $SnCl_4.5H_2O$, and 0-40 cc/min through molten $SbCl_3$. Typical deposition time was 60 minutes which resulted in a film thickness of about 1000-1500 Å. Thin molybdenum masks with circular holes of about 2.0 - 3.0 mm diameter were used to define the area of SnO_2 dots on oxidized silicon samples.

Oxide from the back of the wafer was etched in hydrofluoric acid after protecting the front surface with apiezon wax as described above in case of spray deposited samples. Aluminium was deposited by vacuum evaporation process using a tungsten filament source to form back ohmic contact on the samples.

4.2.3 Fabrication of Electron-Beam Deposited Sn Doped In_2O_3-SiO_2-Si Structures

The starting material were n- and p-type epitaxial silicon wafers with (100) surface orientation and layer resistivity of 1.0 Ohm-cm. The wafer cleaning procedure, including preoxidation and subsequent oxide removal, was same as that described above in case of chemical vapor deposited samples. Final oxidation was carried out in dry oxygen at 1100°C at atmospheric pressure for 30 minutes. No post oxidation annealing was carried out.

Immediately after oxidation, the wafers were introduced into the vacuum chamber of a Varian VT-112B ultrahigh vacuum system,pumped with sorption, sublimation and sputter-ion pumps. This vacuum system was fitted with a Varian three crucible 2 kW electron gun. The details of the e-beam deposition set-up and deposition procedure are given in Chapter 2. After the vacuum chamber was pumped down to 1.0×10^{-7} torr pressure, substrate temperature was raised to 300°C and stabilized. Filtered dry oxygen was then introduced and the partial pressure of oxygen was adjusted to 1.0×10^{-5} torr. Layers of Sn-doped In_2O_3 were deposited on the oxidized silicon substrates by upward electron beam evaporation from indium oxide tablets containing 10 atomic percent tin. The cryo panel was chilled by liquid nitrogen during evaporation and a shutter

was used to protect the substrate from deposition during initial outgassing of the indium oxide tablet. Stainless steel crucibles of the electron gun were cooled by chilled recirculating water. Substrates were located about 17 cm above the In_2O_3 tablets, and were supported on molybdenum masks in a substrate holder. Circular dots of 1.0 mm diameter were deposited through the molybdenum masks and typical deposition time was 60 minutes resulting in the In_2O_3 film thickness of about 2000 Å.

The back contact (Al for n-type and Au for p-type silicon) was formed by filament evaporation in a separate Varian VT-112A ultra high vacuum system after removal of back oxide from substrates as described earlier in case of spray or chemical vapor deposited samples.

4.2.4 Electrical Measurements

Electrical measurements were carried out at room temperature with the samples placed in a light and electrically shielded box. Contact to the transparent gate was made with the help of a fine tipped telescopic spring probe with tip diameter of 0.2 mm. Capacitance-voltage and conductance-voltage characteristics were measured in dark as well as under various levels of illumination over the frequency of 30 Hz - 100 kHz with the help of a General Radio 1616 precision capacitance system, a Keithley 616 digital electrometer, and a finely adjustable dc

power supply. The same at 1 MHz were obtained with the help of a Boonton 75D capacitance bridge, a Keithley 191 digital multimeter, and a finely adjustable dc power supply. The leakage current of the devices were measured as a function of voltage with the help of a Keithley 610C electrometer, a Keithley 191 digital multimeter, and a power supply. Tungsten lamp illumination was used for measurements under optical illumination and the light was allowed into the box through a tiny slit. The area of the transparent gate was measured under a WILD M8 stereo zoom microscope.

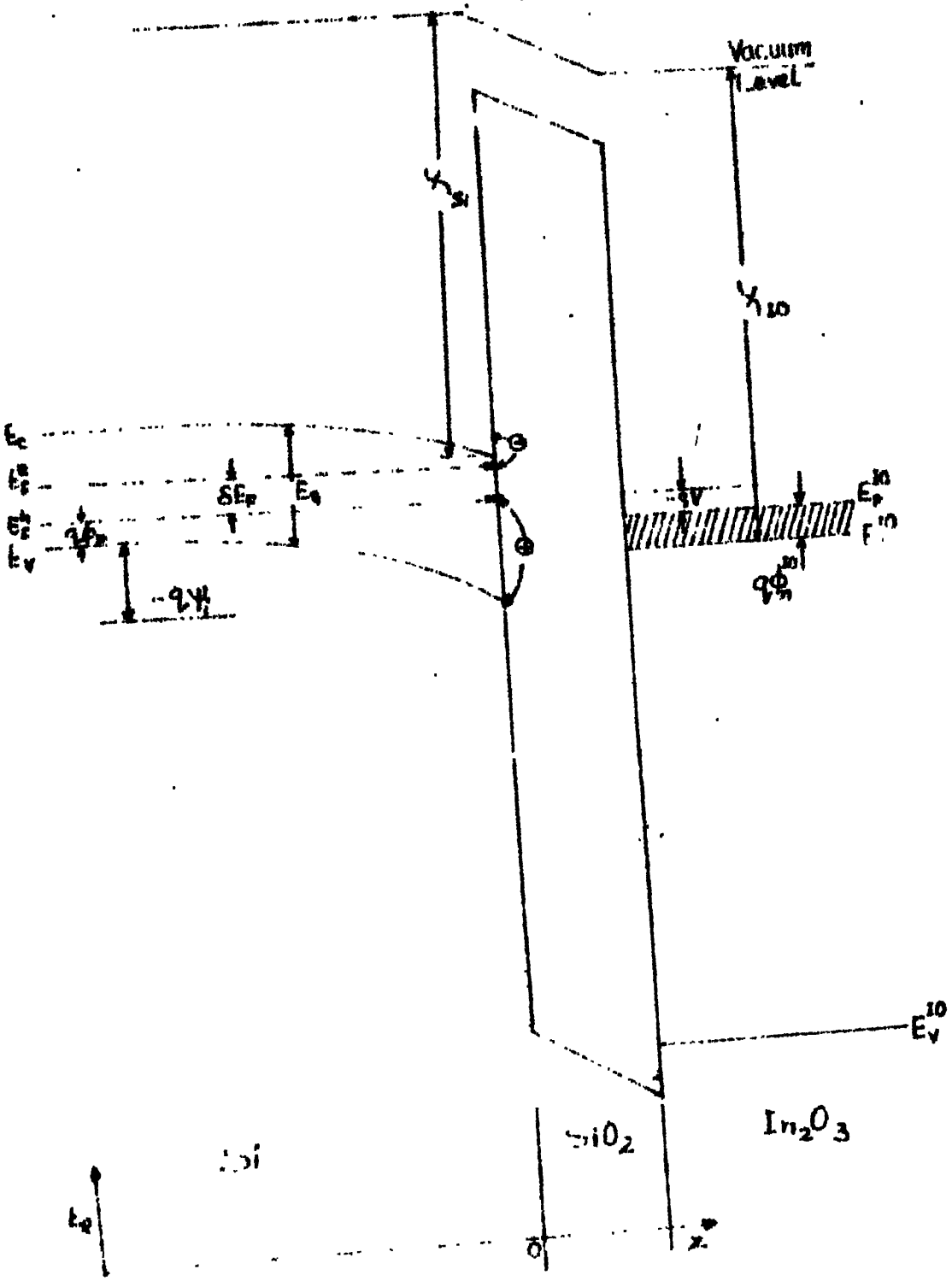
4.3 INTERFACE INVESTIGATION TECHNIQUE USING ADMITTANCE DATA UNDER ILLUMINATION

The technique proposed for interface investigation using surface admittance data of transparent gate MOS structure under illumination, is discussed in this section with the help of an electron-beam deposited In_2O_3-SiO_2-pSi structure, sample EPOI-7. This sample had an oxide thermally grown in dry oxygen at 1100°C for 30 minutes. The capacitance technique consists of measuring high frequency capacitance-voltage characteristics in dark (and under different illumination levels if quasi-Fermi level separation is to be determined from high frequency capacitance data) and measuring low frequency capacitance-voltage characteristics in dark and

under various illumination levels. The conductance technique consists of measuring admittance-voltage characteristics at various frequencies in dark and under the illumination levels used during capacitance measurements, and analysis of measured admittance data. It is to be noted that the capacitance and the conductance as a function of bias at a particular illumination level are measured simultaneously by the bridge.

4.3.1 Capacitance Data Analysis

Figure 4.1 illustrates energy level diagram of a transparent conductor (In_2O_3)-oxide (SiO_2)-semiconductor (p-Si) structure, under light, at a certain bias V. In this energy level diagram, E_c is the silicon conduction band edge, E_v is the silicon valence band edge, E_f^h is the hole imref, E_F^e is the electron imref, E_G is the silicon bandgap, Ψ_i is the interface potential, ϕ_p is the bulk silicon Fermi potential, χ_{Si} is the silicon electron affinity, χ_{IO} is the indium oxide electron affinity, E_f^{IO} is the Fermi level in indium oxide, ϕ_n^{IO} is the bulk indium oxide Fermi potential, E_c^{IO} is the indium oxide conduction band edge, and E_v^{IO} is the indium oxide valence band edge. A small ac signal superimposed on the applied bias causes change in space charge with change in interface potential Ψ_i, and the change in interface state position with respect to the Fermi level position causes charging discharging of interface states. The measured equilibrium (low frequency)



Energy band diagram of a transparent conductor (Indium) oxide (In_2O_3) - semiconductor (p-Si) structure, at a certain bias V, under illumination.

capacitance at any bias is therefore due to contributions from oxide capacitance, space charge capacitance, and interface state capacitance. These capacitances can be resolved with the help of equivalent circuits given in Figure 2 for equilibrium (low) frequency. Figures 2(a), (b) correspond to the dark condition, where C^{d}_{lfd} is the equilibrium low frequency measured capacitance in dark, C^{d}_{scd} is the space charge capacitance in dark, C^{d}_{is} is the capacitance associated with interface states N^{d}_{is} in dark, and C^{p}_{lfd} is the equivalent parallel capacitance due to C_{scd} and C^{d}_{is}. Similarly Figures 2(c),(d) correspond to the illuminated condition, where C_{lfl} is the equilibrium low frequency measured capacitance under illumination, C_{scl} is the space charge capacitance under illumination, C^{l}_{is} is the capacitance associated with interface states N^{l}_{is} under illumination.

In order to find interface state density at a particular surface potential, one needs to know oxide capacitance, C_{ox}, and space charge capacitance, C_{sc}. The oxide capacitance, C_{ox}, is a plane parallel capacitor and depends on the oxide thickness, t_{ox}, and oxide permittivity, ϵ_{ox}:

$$(C_{ox}/A) = \varepsilon_{ox}/t_{ox} = K_{ox}\,\varepsilon_{o}/t_{ox} \qquad (4.1)$$

where A is the area of the plane parallel capacitor (i.e. device area), K_{ox} is the oxide dielectric constant, and ε_{o} is

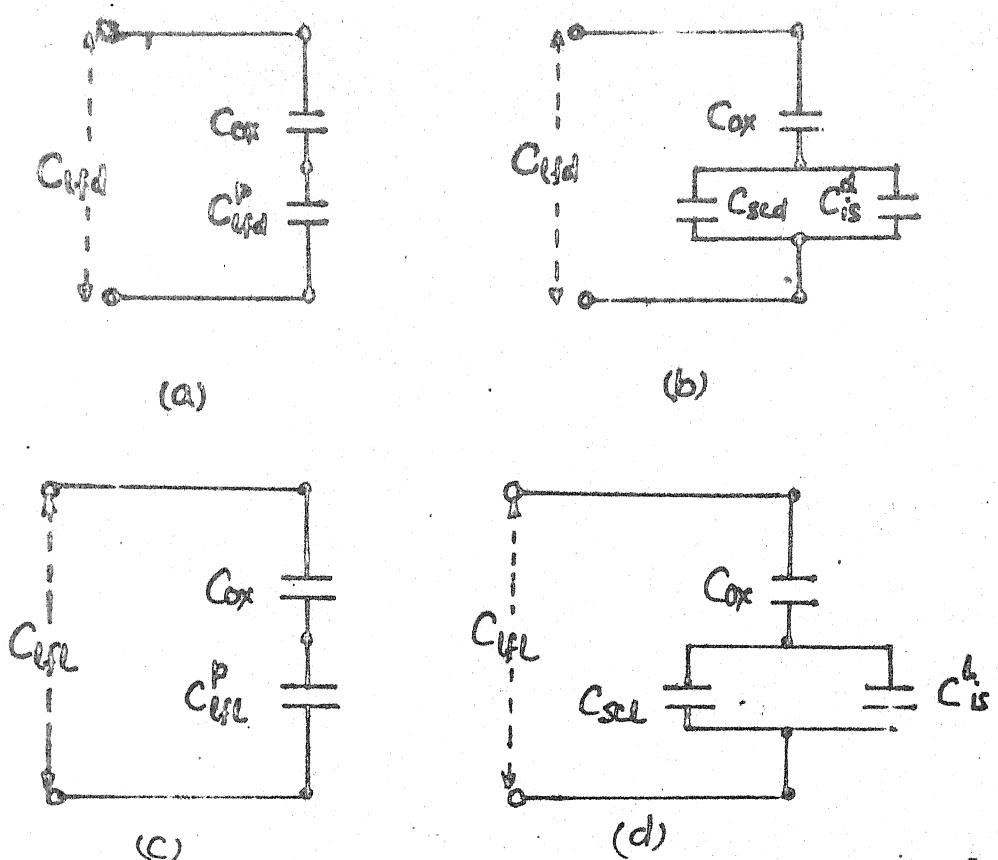


Figure 4.2 Equivalent circuit diagram of In_2O_3-SiO_2-Si Structure at low i.e. equilibrium frequency showing measured capacitance in terms of oxide capacitance, space-charge capacitance, interface state capacitance, and equivalent-parallel capacitance, in dark [(a),(b)] and under illuminated [(c),(d)] conditions.

the permittivity of free space. The value of oxide dielectric constant, K_{ox}, is usually not known for thin and intermediate oxides, and is assumed to be 3.82, its value for thick oxides. Impurities, however, may change its value considerably. The value of oxide capacitance is generally estimated from saturated MOS capacitance in accumulation or in strong inversion at equilibrium low frequency .

The silicon space charge in dark, Q_{scd}, can be found by solving Poisson's equation in the space charge layer. At room temperature and in non-degenerate silicon with constant doping density, the silicon space charge in dark Q_{scd}, is given by the following expressions [1] :

$$\text{(a)}\quad Q_{scd} = \mp \sqrt{(2kT\,\varepsilon_s p_{po})\left[\exp(-U_s)+U_s-1+\left(\frac{n_{po}}{p_{po}}\right)\{\exp(U_s)-U_s-1\}\right]}, \qquad \text{p-Si}$$

$$\text{(b)}\quad Q_{scd} = \mp \sqrt{(2kT\,\varepsilon_s n_{no})\left[\exp(U_s)-U_s-1+(p_{no}/n_{no})\{\exp(-U_s)+U_s-1\}\right]}, \qquad \text{n-Si}$$

$$\text{(c)}\quad p_{po} \simeq N_A, \quad n_{no} \approx N_D, \quad p_{po}\cdot n_{po} = n_{no}\cdot p_{no} = n_i^2 \quad \text{under thermal equilibrium,}$$

$$\text{(d)}\quad U_s = q\,\Psi_i/kT \qquad (4.2)$$

In these equations, k is Boltzmann's constant, ε_s is semiconductor permittivity, $p_{po}(n_{no})$ is majority carrier concentration at the interface, $n_{po}(p_{no})$ is minority carrier concentration at the interface, T is device temperature, $N_A(N_D)$ is doping density in p-type (n-type) silicon, n_i is intrinsic carrier concentration in silicon, and q is magnitude of electronic charge.

The silicon space charge capacitance per unit area, in dark, C_{scd}/A, is obtained by differentiating the space charge, Q_{scd}, with respect to the surface potential, Ψ_i. The silicon space charge capacitance per unit area, C_{scd}/A, is a function of the doping density, N_{doping}, and surface potential, Ψ_i, and can be calculated with the help of following expressions [1] :

$$(a)\ \left(\frac{C_{scd}}{A}\right) = \frac{dQ_{scd}}{d\,C_i} = \pm\ \left[(p_{po}q^2\varepsilon_s)/(2kT)\right] \cdot \frac{\left[1-\exp(-U_s) + (n_{po}/p_{po})\{\exp(U_s)-1\}\right]}{\sqrt{\exp(-U_s)+U_s-1+(n_{po}/p_{po})[\exp(U_s)-U_s-1]}},\quad \text{p-Si}$$

$$(b)\ \left(\frac{C_{scd}}{A}\right) = \pm\sqrt{\left[n_{no}\cdot q^2\ \varepsilon_s\right)/(2kT)]} \cdot \frac{\left[\exp(U_s)-1-(p_{no}/n_{no})\{\exp(-U_s)-1\}\right]}{\sqrt{\exp(U_s)-U_s-1+(p_{no}/n_{no})\{\exp(-U_s)+U_s-1\}}},\quad \text{n-Si}$$

(4.3)

The upper sign in these expressions is valid for $\Psi_i > 0$, i.e., downward bending, and the lower sign for $\Psi_i < 0$, i.e., upward bending of the energy bands.

The onset of strong inversion in dark takes place at interface potential, Ψ_i^{invd}, given by the expression :

$$
\begin{aligned}
&(a)\ \Psi_i^{invd} = V_G - 2\phi_p\ , && \text{p-Si} \\
&(b)\ \phi_p = \left(\frac{kT}{q}\right) \ln\left(N_V/N_A\right), && \text{p-Si} \\
&(c)\ \Psi_i^{invd} = V_G - 2\phi_n, && \text{n-Si} \\
&(d)\ \phi_n = \left(\frac{kT}{q}\right) \ln\left(N_C/N_D\right), && \text{n-Si}
\end{aligned}
\qquad (4.4)
$$

V_G is the voltage equivalent of silicon band gap E_G, $\phi_p(\phi_n)$ is Fermi level potential in p-type (n-type) silicon, $N_V(N_C)$ is effective density of states in valence band (conduction band), and $N_A(N_D)$ is silicon doping density in p-type (n-type) silicon.

Figure 4.3 contains a selection of measured capacitance-voltage characteristics of In_2O_3-SiO_2-Si structure, sample EPOI-7. The 30 Hz characteristics obtained in dark and under three illumination levels L_1, L_2 and L_3, and the dark 100 kHz characteristics have been included in Figure 4.3. The lowest illumination level, L_1, was so chosen that there was no dispersion in strong inversion region below 30 Hz frequency. This

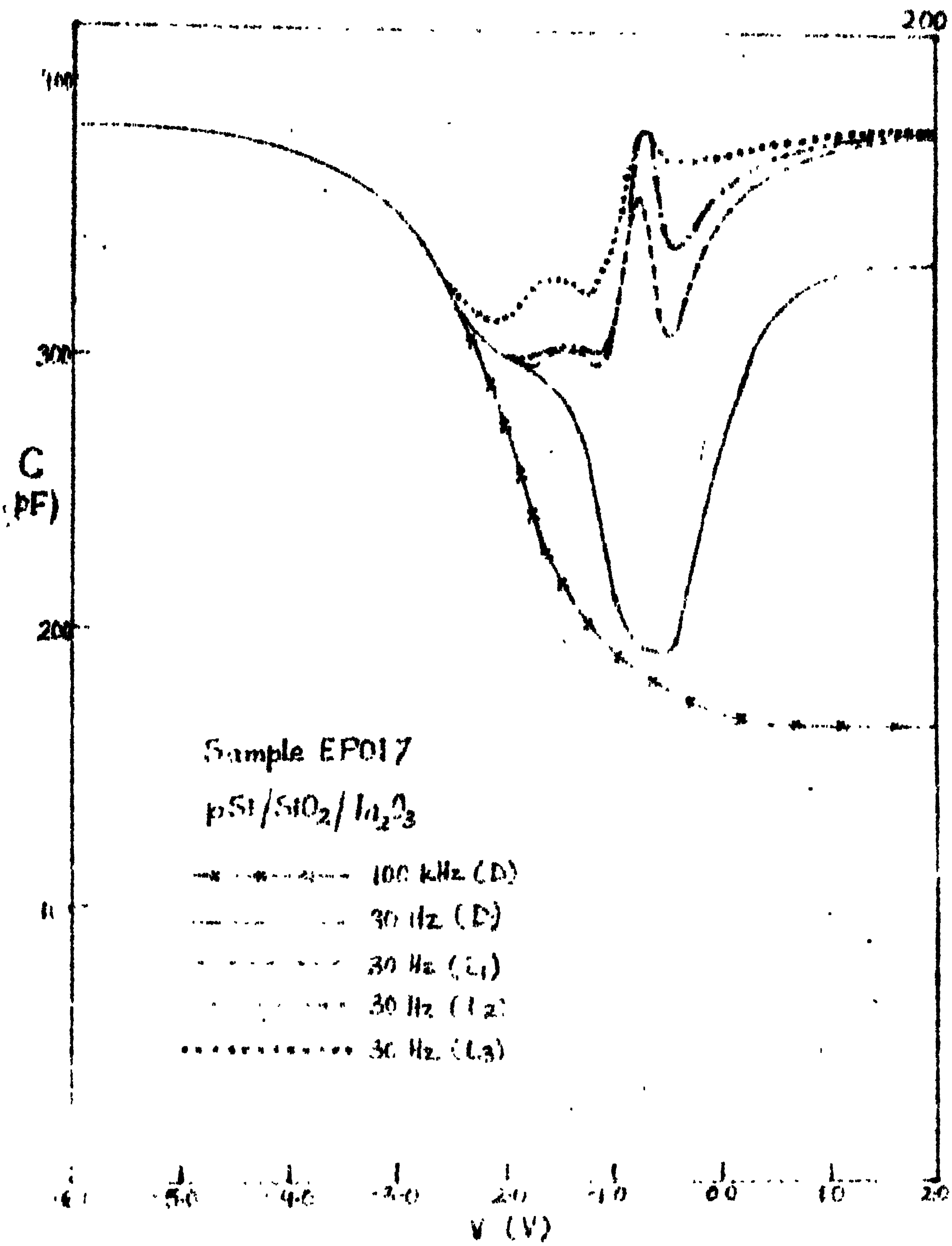


Figure 4.4 A selection of capacitance-voltage (C-V) characteristics of a typic[illegible] deposited by [illegible] device, sample EP017, measured at different frequencies and in dark and under illumination levels L1, L2 and L3.

ensured that the low frequency equilibrium capacitance-voltage characteristics were obtained and both the inversion layer as well as the interface states responded to the applied small sinusoidal signal. In dark, equilibrium was not obtained at 30 Hz between both, the inversion layer and a part of the interface states, and the small ac signal. Under optical illumination, at levels L_1 and above, the device capacitance saturated to the silicon oxide capacitance, both in strong accumulation and is strong inversion. This fact supports the assumption that the energy bands are flat in transparent conductor and TCOS structure can be used for interface investigation using small signal admittance measurements as in case of MOS structure. The silicon oxide thickness, t_{ox}, was calculated using Equation (4.1) and its value came out to be 678 Å. The experimental data of Figure 4.3 indicate the presence of two peaks in the interface state profile, one near the valence band edge, and the other near the conduction band edge.

At 100 kHz, the measured capacitance in dark, C_{hfd}, will not have contribution from interface states in strong inversion. The processing of the measured capacitance data begins with the calculation of the doping density, N_{doping} (N_A or N_D), from the high frequency minimum MOS capacitance, C_{hfd}^{min}, measured at high frequency in dark in strong inversion where capacitance value becames constant, using the following relations :

$$(a) \quad 1/C_{scd}^{min} = 1/C_{hfd}^{min} - 1/C_{ox} \qquad (4.5)$$

$$(b) \quad N_{doping} = 2\left(\frac{C_{scd}^{min}}{A}\right)^2 \Psi_i^{invd}/q\,\varepsilon_s$$

Here C_{scd}^{min} is the minimum value of space charge capacitance in dark under strong inversion, and the interface potential at the onset of strong inversion in dark, Ψ_i^{invd}, is defined by Equation(4.4). For sample EPOI-7, the value of oxide capacitance was estimated from the saturated low frequency MOS capacitance of Figure 4.3 in strong inversion. The exact value of doping density near the interface, N_{doping}, was found by a few iterations using Equations(4.4 a , b) and(4.5 b). The value of the acceptor density in case of sample EPOI-7 came out to be $1.25 \times 10^{16} cm^{-3}$, while its bulk value according to resistivity was $1.60 \times 10^{16} cm^{-3}$.

Using the experimentally obtained doping density, the dark space charge capacitance, C_{scd}, was calculated as a function of interface potential, Ψ_i, using Equation(4.3 a). Calculated C_{scd} was then plotted semilogarithmically as a function of interface potential, Ψ_i, and such a plot for sample EPOI-7 is shown in Figure 4.4.

The low frequency dark MOS capacitance measured at 30 Hz, C_{lfd}, was then reduced to the parallel capacitance, C_{lfd}^{p}, defined by the equivalent circuit diagram of Figures 4.2(a),(b), and according to the relation :

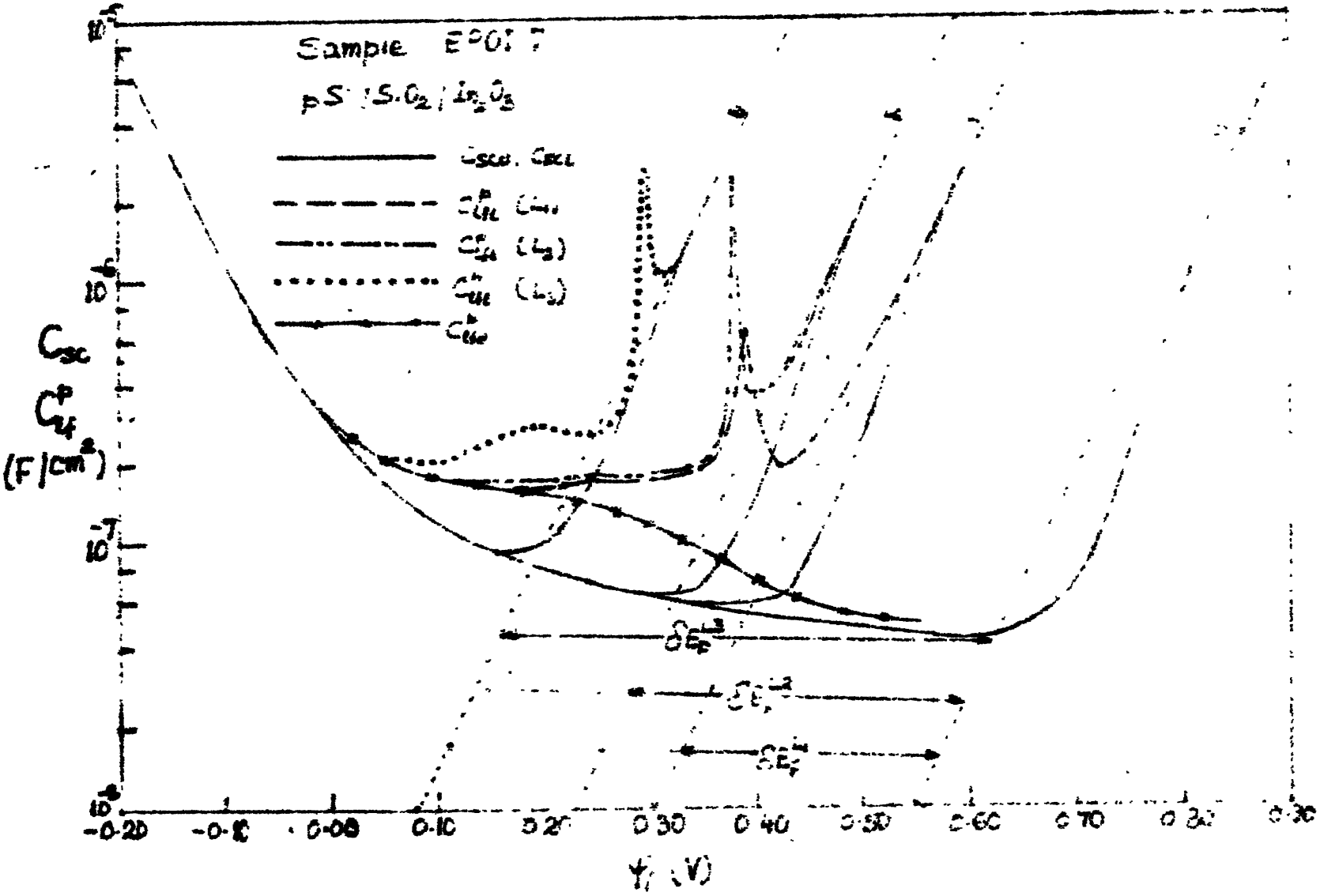


Figure 4.4 Semilogarithmic plots of experimental C_{sc} vs ψ_i and calculated C_{sc} vs ψ_i characteristics of Sn in EPOI-7 in dark, and under illumination levels L_1, L_2, and L_3

$$1/C^{p}_{lfd} = 1/C_{lfd} - 1/C_{ox} \qquad (4.6)$$

and the value for C^{p}_{lfd} at each bias was calculated.

In the next step, the interface potential, ψ_i, as a function of applied bias, V, was obtained in dark by graphically integrating the low frequency capacitance-voltage characteristics, measured at 30 Hz, according to the relation [16] :

$$\Psi_i = \int[1-(C_{lfd}/C_{ox})]dv + K \qquad (4.7)$$

where K is the integration constant. Accurate values of the integration constant and the oxide capacitance can be obtained in the following manner. Initially the graphical integration of low frequency C-V curve is carried out using Equation(4.7) in the accumulation region and simultaneously the equivalent parallel capacitance in dark, C^{p}_{lfd} is calculated using Equation(4.6). Generally, in strong accumulation, the parallel capacitance, C^{p}_{lfd}, can be expected to consist mainly of the space charge capacitance C_{scd}. In that case, if the oxide capacitance is optimally estimated, the experimental ln C^{p}_{lfd} vs Ψ_i relation should come out to be linear with the slope of q/2kT; since in strong accumulation, the expression for C_{scd} given by Equation(4.3)can be approximated as :

$$\text{(a)}\quad \frac{C_{scd}}{A} \simeq [q^2 \varepsilon_s N_A/2kT]^{1/2} [\exp(-U_s/2)], \text{p-Si, strong accumulation}$$

$$\text{(b)}\quad \frac{C_{scd}}{A} \simeq [q^2 \varepsilon_s N_D/2kT]^{1/2} [\exp(U_s/2)], \text{n-Si, strong accumulation} \qquad (4.8)$$

A few iterations to find the correct slope of ln C^p_{lfd} vs Ψ_i curve in strong accumulation will lead to very accurate determination of oxide capacitance. Now the linear part of the experimental ln C^p_{lfd} vs Ψ_i relation can be matched against the calculated ln C_{scd} vs Ψ_i characteristic in strong accumulation to obtain the integration constant of Equation (4.7).

Once values of the oxide capacitance and the integration constant of Equation (4.7) were optimized, values of C^p_{lfd} and Ψ_i were calculated over the whole region of measurement, and ln C^p_{lfd} vs Ψ_i was plotted as shown in Figure 4.4. Figure 4.5 shows the experimentally obtained Ψ_i vs V characteristics, in dark and under illumination levels L_1, L_2 and L_3, for sample EPOT-7. The dark C-V characteristics measured at 30 Hz exhibited dispersion in inversion, i.e., beyond -0.75V. C^p_{lfd} was not calculated in the region of inversion showing dispersion. Subsequently, the interface state density in dark, N^d_{is} was obtained at various interface potentials, Ψ_i, using the relation :

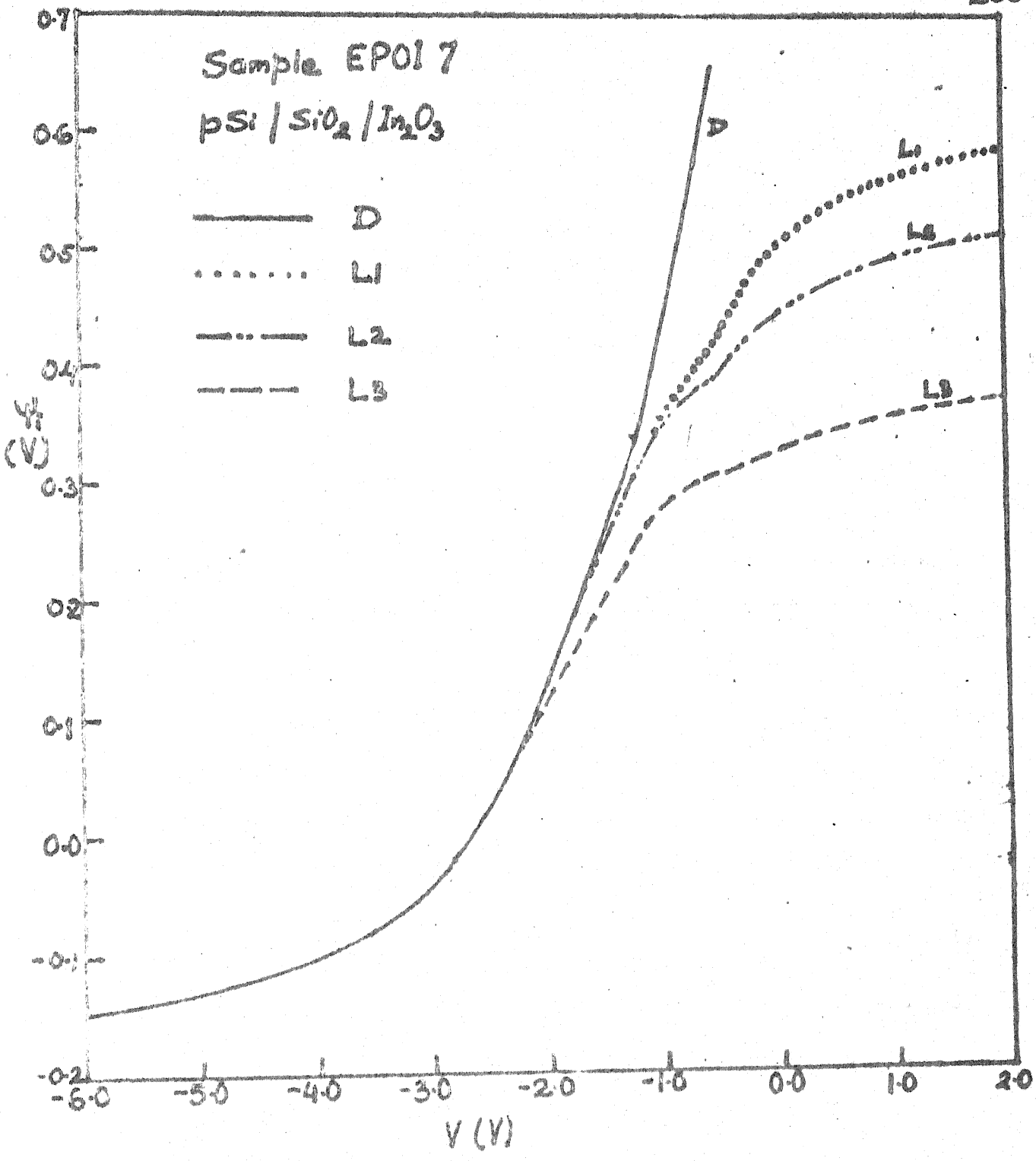


Figure 4.9 Experimental ψ_s vs V characteristics of sample EP01-7 obtained from graphical integration of low frequency C-V characteristics in dark and under illumination levels L_1, L_2, and L_3

$$N_{is}^{d} = C_{is}^{d}/q.A = (C_{lfd}^{p}-C_{scd})/q.A \qquad (4.9)$$

The band energy, E, corresponding to interface potential, ψ_i, in dark is given by :

$$\begin{aligned}
&(a) \quad E-E_V = q(\phi_p + \Psi_i) && p\text{-Si} \\
&(b) \quad E_c-E = E_G-q(\phi_p + \Psi_i) && p\text{-Si} \\
&(c) \quad E_C-E = q(\phi_n - \Psi_i) && n\text{-Si} \\
&(d) \quad E-E_v = E_G-q(\phi_n - \Psi_i), && n\text{-Si}
\end{aligned} \qquad (4.10)$$

The interface state density profile in dark as a function of band energy was obtained for sample EPOI-7 using Equations (4.9),(4.10) and has been displayed in Figure 4.6.

The capacitance data under light can be analysed in the following manner. The low frequency parallel capacitance under light, C_{lfl},can be obtained according to the equivalent circuit diagrams of Figures 4.2(c),(d) and the relation :

$$1/C_{lfl}^{p} = 1/C_{lfl} - 1/C_{ox} \qquad (4.11)$$

C_{lfl} is the low frequency or the equilibrium MOS capacitance under light. The experimental interface potential vs bias relation, under a particular illumination level, can be obtained by graphically integrating the corresponding low frequency equilibrium MOS capacitance vs voltage (C_{lfl}-V) characteristics according to the relation :

$$\Psi_i = \int[1-(C_{lfl}/C_{ox})]\, dV + K \qquad (4.12)$$

Same value of the integration constant can be used as found for the dark condition, if the levels of illumination do not exceed low level injection conditions, as was the case in the present investigation.

At illumination level L_1 equilibrium was achieved at and below the frequency of 30 Hz, at illumination level L_2 below 120 Hz, and at L_3 below 400 Hz. This shows that under light one is not required to go to very low frequencies to obtain equilibrium, and the equilibrium frequency increases with illumination level. Hence, at all the illumination levels, that the device EPOI-7 was subjected to, the 30 Hz capacitance-voltage (C_{lfl}-V) characteristics can be considered to be under equilibrium condition. The experimental ln C^p_{lfl} vs Ψ_i characteristics obtained using Equations (4.11) and (4.12), at illumination levels L_1, L_2 and L_3 have been displayed in Figure 4.4.

The silicon space charge capacitance under a given illumination level, C_{scl}, can be calculated using experimental values of the doping density and the quasi-Fermi level separation, δE_F, with the help of following relations, as was done in dark :

$$(a)\quad \frac{C_{scl}}{A} = \pm \sqrt{(p^1_{po}\cdot q^2\cdot \varepsilon_s)/(2kT)}\;\frac{[1-\exp(-U_s)+(n^1_{po}/p^1_{po})\{\exp(U_s)-1\}]}{\sqrt{\exp(-U_s)+U_s-1+(n^1_{po}/p^1_{po})[\exp(U_s)-U_s-1]}},\ \text{p-Si}$$

$$(b)\quad \frac{C_{scl}}{A} = \pm \sqrt{(n^1_{no}\, q^2\, \varepsilon_s)/(2kT)]}\;\frac{[\exp(U_s)-1-(p^1_{no}/n^1_{no})\{\exp(-U_s)-1\}]}{\exp(U_s)-U_s-1+(p^1_{no}/n^1_{no})[\exp(-U_s)+U_s-1]},\ \text{n-Si}$$

$$(c)\quad p^1_{po} \simeq p_{po} = N_A,\ n^1_{no} \approx n_{no} \simeq N_D,\ \text{under low level injection}$$

$$(d)\quad n^1_{po} = n_{po}\exp(|\delta E_F|/kT),\ \text{p-Si}$$

$$(e)\quad p^1_{no} = p_{no}\exp(|\delta E_F|/kT),\ \text{n-Si} \qquad (4.13)$$

Comparison of Equation (4.13) with Equation(4.3),reveals that space charge capacitance under light, C_{scl}, will be same as that under dark, C_{scd}, except in the region of strong inversion, where C_{scl} differs by a factor of $\exp(\delta E_F/2kT)$ in numerator of expression for C_{scd}.

To calculate space charge capacitance under light, C_{scl}, using Equations (4.13 a - e), the quasi-Fermi level separation under the respective levels of illumination have to be known. The imref separation can be obtained in three different ways, namely, from the measured high frequency illuminated capacitance

minimum in strong inversion, or from graphical integration of the measured low frequency illuminated C-V characteristics, or from the parallel shift of the experimental ln C^{p}_{lfl} vs Ψ_i characteristic in strong inversion.

Under illumination, strong inversion sets in at a different value of interface potential, Ψ_i^{invl}, which can be obtained from the measured high frequency minimum MOS capacitance under illumination, C^{min}_{hfl}, using the relations :

$$\text{(a)} \quad 1/C^{min}_{scl} = 1/C^{min}_{hfl} - 1/C_{ox}$$

$$\text{(b)} \quad \Psi_i^{invl} = q\,\varepsilon_s\, N_{doping}/2(C^{min}_{scl}/A)^2 \qquad (4.14)$$

In the dark condition, the interface potential at the onset of strong inversion, Ψ_i^{invl}, is given by Equation(4.4 a , c). However, under illumination, the quasi-Fermi level separation, δE_F, reduces the band bending (interface potential) required to set in strong inversion. The difference in the values of the interface potential required for strong inversion to set in, in dark and under illumination, gives quasi-Fermi level separation :

$$\delta E_F = q\,|\,\Psi_i^{invd} - \Psi_i^{invl}\,| \qquad (4.15)$$

The graphical integration of low frequency equilibrium C-V characteristic gives value of interface potential as a function of voltage given by Equations(4.7)and(4.12)for dark

and illuminated conditions respectively. If such graphical integration is carried out between points in strong accumulation and very strong inversion in dark, where $C_{lfd}/C_{ox} \simeq 1.0$, then the interface potential scans practically the whole band gap. However, under illumination, strong inversion sets in at a lower value of interface potential by an amount $\delta E_F/q$. Hence, graphical integration of C_{lfl} vs V characteristic between very strong inversion and strong accumulation, so that $C_{lfl}/C_{ox} \simeq 1$, can give quasi-Fermi level separation by following relations :

$$(a) \quad \Sigma \Psi_i^l = \int_{C_{lfl}/C_{ox}=1}^{C_{lfl}/C_{ox}=1} [1-(C_{lfl}/C_{ox})]dV, \qquad (4.16)$$

$$(b) \quad \delta E_F = E_G - q(\Sigma \Psi_i^l)$$

$\Sigma \Psi_i^l$ is the integrated value of interface potential between strong accumulation and very strong inversion obtained from low frequency C-V characteristic under light.

Perhaps the most accurate way of determining δE_F is to determine the parallel shift between the experimental ln C_{lfl}^p vs Ψ_i characteristic and the calculated ln C_{scd} vs Ψ_i characteristic in strong inversion, as shown in Figure 4.4. In very strong inversion, the low frequency parallel capacitance, C_{lfl}^p reduces to space charge capacitance, C_{scl} under illumination, since $C_{is}^l \ll C_{scl}$. Equations(4.13 a , c) can then be approximated as :

$$\text{(a)}\quad C^{p}_{lfl} \simeq C_{scl} \simeq A(q^2 \varepsilon_s n_{po}/2kT)^{1/2} \cdot \exp[(q\Psi_i + \delta E_F)/2kT] \quad , \quad \text{p-Si}$$

$$\text{(b)}\quad C^{p}_{lfl} \simeq C_{scl} \simeq A(q^2 \varepsilon_s p_{no}/2kT)^{1/2} \cdot \exp[(-q\Psi_i + \delta E_F)/2kT] \quad , \quad \text{n-Si} \qquad (4.17)$$

Equation(4.17) shows that $\ln C^{p}_{lfl}$ vs Ψ_i would be linear in strong inversion with a slope equal to q/2kT, and will have a parallel voltage shift of $\delta E_F/q$ from the calculated space charge capacitance in dark C_{scd}. As illumination level increases, as in case of sample EPOI-7 from L_1 to L_3, corresponding quasi-Fermi level separation increases and $\ln C^{p}_{lfl}$ vs Ψ_i curves with increasing illumination will show a parallel voltage shift in strong inversion towards flat band condition.

Values of quasi-Fermi level separation, corresponding to illumination leads L_1, L_2 and L_3 for sample EPOI-7, obtained by three different experimental techniques proposed, have been presented in Table 4.1.

Once quasi-Fermi level separation at each illumination level is obtained from any of the methods proposed above, space charge capacitance under illumination, C_{scl}, can be calculated using Equation(4.13). Figure 4.4 displays the illuminated $\ln C_{scl}$ vs Ψ_i characteristics corresponding to different

Table 4.1 : Experimental values of imref separation obtained, under different illumination levels, from different techniques for sample EPOI-7

Illumination level	δE_F (eV)		
	From graphical integration of C_{lfl} vs V curve	From high frequency capacitance minimum	From parallel shift of ln C_p^l vs i curve in strong inversion
L_1	0.24	0.27	0.25
L_2	0.31	0.34	0.32
L_3	0.46	0.47	0.47

illumination levels L_1,L_2, and L_3. Subsequently, magnitude of the experimentally obtained interface state density, N^l_{is}, corresponding to a particular illumination level, at different values of interface potential, were obtained by using the relation :

$$N^l_{is} = (C^p_{lfl}-C_{scl})/qA \qquad (4.18)$$

Before the energy location of the interface state could be ascertained from illuminated capacitance measurements, it becomes necessary to determine for which values of the interface potential, the electron imref, E^e_F, controls interface state occupancy, and for which values, the hole imref, E^h_F, controls the same. If the state capture cross-section is same for electrons and holes, and if the capture cross-section is independent of energy level, this issue can be resolved easily. In that case, the electron quasi-Fermi level will control state occupancy, if at the interface, $(E_c-E^e_F)$ is smaller than $(E^h_F-E_v)$; otherwise the hole quasi-Fermi level will control the state occupancy, cf. Fig. 4.1. In other words, if for p-type silicon, the condition

$$[V_G-(\Psi_i+\phi_p+\delta E_F/q)] < (\Psi_i+\phi_p) \qquad (4.19)$$

prevails, charge exchange will take place mainly between interface states at the electron imref and the conduction

band; otherwise, between interface states at the hole imref and the valence band.

In many real interfaces, the electron capture cross-section, σ_e, may differ by orders of magnitude from the hole capture cross-section, σ_h, of an interface state, and/or, the capture cross-section may vary strongly with the energy level of the state. In such a situation, if

$$n_s \cdot \sigma_e >> p_s \cdot \sigma_h \qquad (4.20)$$

charge exchange with states around electron imref, E_F^e, will dominate, otherwise with states around hole imref, E_F^h. n_s and p_s are the electron and hole concentrations at the interface respectively. If the capture cross-sections are independent of band gap energy, then the condition of Equation (4.20) can be translated into the following one, in terms of the interface potential, for p-type silicon :

$$(V_G - \Psi_i - \phi_p - \frac{\delta E_F}{q}) < [\Psi_i + \phi_p - \frac{kT}{q} \ln(\frac{\sigma_h}{\sigma_e})] \qquad (4.21)$$

Should the capture cross-section vary with the state energy level, the situation becomes more complicated. In this case, capture cross-sections have to be determined in different regions of the bandgap, and then $n_s \cdot \sigma_e$ has to be compared with $p_s \cdot \sigma_h$ for each value of the interface potential, to determine which imref controls interface state occupancy at the particular interface potential, and contributes to interface state admittance.

In case information about σ_h and σ_e cannot be obtained experimentally, the region of interface potential where uncertainity about the dominant imref prevails, will at the most be about 0.12V on each side of the interface potential which makes quasi-Fermi levels equidistant from the midgap. This is based on the assumption that the capture cross-sections may not differ by more than four orders of magnitude, in which case the maximum region of uncertainity in interface potential region will be $|\frac{kT}{q} \ln(\sigma_h/\sigma_e)|$. In such a case, the state density profile was not evaluated in this region of interface potential. States near a band edge were assumed to exchange charge with the corresponding band. If a peaked state density distribution (i.e. peaked C^p_{lfl} vs Ψ_i characteristics) is obtained such that the peak location is outside the above mentioned uncertainity region, the resolution of issue electron vs hole exchange with states is carried out in the following manner. All the states under the peaked state density distribution were assumed to exchange charge with the band whose edge was closer to the observed peak location. For example ln C^p_{lfl} vs Ψ_i characteristic of sample EPOI-7 under illumination level L_1 showed a peaked C^p_{lfl} distribution with the peak located at $\Psi_i = 0.39V$ (cf. Figure 4.4). The imrefs were equidistant from the mid gap at interface potential of 0.26V. Hence all the states giving rise to the peaked C^p_{lfl} distribution with peak located at 0.39V were assumed to exchange charge with conduction band.

Once the dominant imref is identified, at a particular value of the interface potential, the energy location of the state can be determined according to the following relations, for p-type silicon :

(a) $E-E_V = q(\phi_p + \Psi_i)$, if hole imref controls state occupancy,

(b) $E-E_V = E_G - q(\phi_p + \Psi_i) - \delta E_F$, if electron imref controls state occupancy

(4.22)

The preceding discussion underscores the fact that, although the low frequency capacitance technique can be employed independent of the conductance technique to obtain the state density profile from surface admittance measurements in dark, both the techniques have to be employed in order to accurately process illuminated admittance measurements.

Values of electron and hole capture cross-sections, for sample EPOI-7, were obtained over different regions of the silicon bandgap from the conductance technique, which is elaborated in next section. Capture cross-sections were found to vary with the bandgap energy as well as illumination level, and the electron capture cross-sections were found to be orders of magnitude smaller than the hole capture cross-sections. Using experimental values of electron capture cross-section, σ_e, and hole capture cross-section, σ_h, the dominant imref was found at each value of interface potential, and the energy location of

the states were determined. The experimental interface state profile, obtained under illumination levels L_1,L_2 and L_3, by illuminated capacitance data analysis discussed above, have been displayed in Figure 4.5.

4.3.2 Conductance Data Analysis

The measured capacitance of a device consists of oxide capacitance, space charge capacitance, and interface state capacitance. The interface state capacitance is to be extracted from measured capacitance as discussed earlier, and any error involved in determining oxide capacitance and space charge capacitance (or in doping density) may result in inaccuracy in interface state density, especially if it is low. Moreover, the change in capacitance with voltage may not be very large, and hence capacitance measurements have to be very accurate. Conductance is measured simultaneously with capacitance in a standard capacitance bridge. Conductance-voltage characteristics at different frequencies may show peaks whose magnitude may vary by more than one order of magnitude, and hence the peak magnitude and location can be determined easily. Since measured conductance peaks are directly related to the interface states, the information on interface states obtained from conductance measurements are more accurate and reliable, especially when interface state densities are low as in case of thermally oxidized SiO_2-Si systems. However, conductance data analysis is quite involved and is the main drawback of this technique.

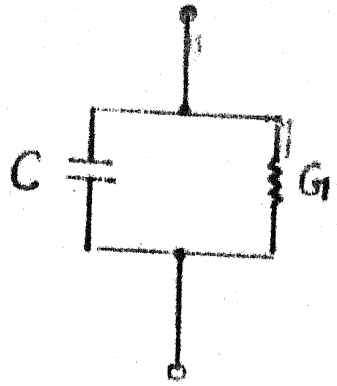
A comprehensive discussion of the conductance technique is given by Nicollian and Goetzberger [19]. The principle of MOS conductance technique can be understood with the help of equivalent circuit diagrams of Figure 4.7. Values of the parallel capacitance C_p and the parallel conductance G_p can be calculated from the measured values of the oxide capacitance, C_{ox}, and the total MOS capacitance, C, and the total MOS conductance, G, using the equivalent circuit diagrams of Figures 4.7(a),(b),(c) and the following relations [19] :

$$(a)\quad C_p = \frac{C_{ox}^2(G^2+\omega^2C^2)[\omega^2C(C_{ox}-C)-G^2]}{\omega^2C_{ox}^2G^2+[\omega^2C(C_{ox}-C)-G^2]^2}$$

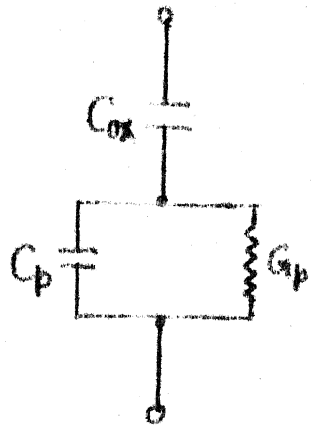
$$(b)\quad G_p = \frac{\omega^2C_{ox}^2G(G^2+\omega^2C^2)}{\omega^2C_{ox}^2G^2+[\omega^2C(C_{ox}-C)-G^2]^2} \qquad (4.23)$$

Here ω is angular frequency of applied ac signal. The observed admittance behaviour can be explained with the help of three different models for equivalent circuit diagrams representing interface states. These models are for single level states, continuum of states, and continuum of states under the influence of statistical potential fluctuations at the interface.

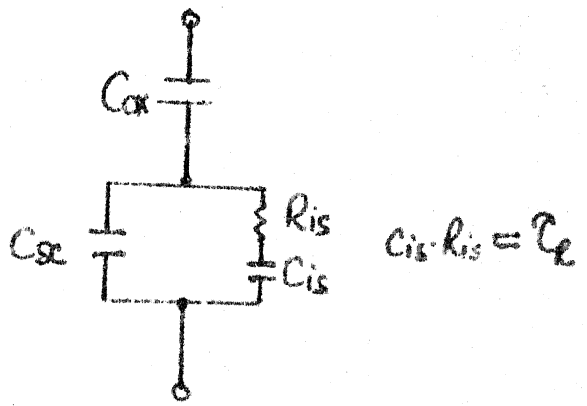
According to Nicollian and Goetzberger [19], charge exchange between the interface state and the majority carrier band is likely to prevail, even in the inversion regime, in dark. Hence the observed conductance peaks in dark arise due to charge exchange between majority carrier band and interface states. If



(a)



(b)



(c)

Figure 4,7 Equivalent circuit diagram of In_2O_3-SiO_2-Si at an intermediate frequency

C_{is} is the interface state capacitance and R_{is} is the resistance associated with those states, then the product $C_{is}R_{is}$ gives interface recombination time constant for majority carriers, τ_R^{maj}, which varies with surface potential, Ψ_i.

For a single level state, interface recombination admittance contains one $C_{is}R_{is}$ branch in equivalent circuit. The frequency dependent equivalent parallel capacitance, C_p, and conductance, G_p, are then given by [19] :

$$\text{(a)}\quad C_p = C_{sc} + \frac{C_{is}}{[1+\omega^2 \tau_R^{maj2}]} \qquad (4.24)$$

$$\text{(b)}\quad G_p = C_{is}\ \omega^2 \tau_R^{maj} /[1+\omega^2 \tau_R^{maj2}]$$

$G_{p/\omega}$ if plotted against frequency or bias goes through a peak at $\omega \tau_R^{maj} = 1$ [19] :

$$\text{(a)}\ \omega\ \tau_R^{maj} = 1 \quad , \text{ at } G_{p/\omega} \text{ peak} \qquad (4.25)$$

$$\text{(b)}\ [G_{p/\omega}]_{max} = \frac{C_{is}}{2} = \frac{q \cdot A \cdot N_{is}}{2}$$

where $[G_{p/\omega}]_{max}$ is its value at peak, A is sample area, C_{is} is interface state capacitance, N_{is} is interface state density, and q is magnitude of electronic charge.

If the states are so close to each other that a continuum of states exists, and their density varies slowly wit surface

potential, then interface recombination admittance contains a number of series $C_{is}R_{is}$ branches which can be grouped together to give majority carrier time constant, τ_R^{maj}. In such a case, C_p and G_p are given by [19] :

$$(a)\quad C_p = C_{sc} + \frac{q.A.N_{is}}{\tau_R^{maj}} \{\tan^{-1}[\omega \tau_R^{maj}]\} \qquad (4.26)$$

$$(b)\quad G_p = \{\frac{q.A.N_{is}}{2\tau_R^{maj}}\} \{\ln[1+\omega^2 \tau_R^{maj2}]\}$$

In case of continuum of states also, $G_{p/\omega}$ shows a peak if plotted against bias or frequency, when [19] :

$$(a)\quad \omega\ \tau_R^{maj} = 1.95 \quad \text{at } G_{p/\omega} \text{ peak} \qquad (4.27)$$

$$(b)\quad [G_{p/\omega}]_{max} = [\frac{q.A.N_{is}}{2}]\ 0.805$$

Statistical fluctuation in surface potential may arise due to random distribution of charges in the oxide, ionized impurities in silicon, and oxide thickness variation over interface plane. In such a case, the parallel capacitance and conductance as functions of average surface potential, Ψ_i, are given by [19] :

$$(a)\ C_p = C_{sc} + \frac{qAN_{is}}{\sqrt{[2\pi(\sigma_s^2+\sigma_B^2+\sigma_x^2)]}} \int_{-2U_B}^{2U_B} [\exp(-Z-y)](\tan^{-1}[\exp(y)])\, dU_s,$$

$$(b)\ G_p = \frac{\omega qAN_{is}}{\sqrt{[2\pi(\sigma_s^2+\sigma_B^2+\sigma_x^2)]}} \int_{-2U_B}^{2U_B} [\exp(-Z-y)]\ (\ln[1+\exp(2y)])dU_s,$$

$$(c)\ y = \ln(\omega\, \tau_R^{maj}),$$

$$(d)\ Z = [(U_s-\bar{U}_s)^2]/[2(\sigma_s^2+\sigma_B^2+\sigma_x^2)],$$

$$(e)\ \bar{U}_s = q\,\bar{\Psi}_i/kT,$$

$$(f)\ U_B = q\,\Psi_B/kT, \qquad (4.28)$$

where $q\,\Psi_B$ is the separation between mid-gap energy level and Fermi level, and σ_s, σ_B, and σ_x are standard deviations given by [19] :

$$(a)\ \sigma_s = \frac{q\ t_{sc}}{kT\ \varepsilon_s[1+C_{ox}/C_{sc}]} \sqrt{\frac{qQ}{\alpha}}$$

$$(b)\ \sigma_B = \frac{q^2\ [N_A\ t_{sc}]^{1/2}\ [1-\exp(-\bar{U}_s)]}{[2kT]\ \varepsilon_s[1+C_{ox}/C_{sc}]}, \text{ for p-Si} \qquad (4.29$$

$$(c)\ \sigma_B = \frac{q^2[N_D\ t_{sc}]^{1/2}\ [\exp(\bar{U}_s)-1]}{[2kT]\ \varepsilon_s[1+C_{ox}/C_{sc}]}, \text{ for n-Si}$$

(d) $$\sigma_x = \frac{q^2 N_A\, t_{sc}^2 [1-\exp(-\bar{U}_s)]}{kT\, \varepsilon_{ox}\, [A/C_{ox}+A/C_{sc}]}, \quad \text{for p-Si}$$

(e) $$\sigma_x = \frac{q^2 N_D\, t_{sc}^2\, [\exp(\bar{U}_s)-1]}{kT\, \varepsilon_{ox}\, [A/C_{ox}+A/C_{sc}]}, \quad \text{for n-Si,}$$

(f) $$t_{sc} = A\, \varepsilon_s / C_{sc},$$

(g) $$\alpha \approx 1.5\, t_{sc},$$

(h) $$Q = (C_{ox}/A)\, [-V+\bar{\Psi}_i)] - Q_{sc}$$

For all values of oxide thickness, σ_x is smaller than σ_s and σ_B, and in general σ_s is the controlling factor. In case of statistical fluctuation in surface potential also, $G_{p/\omega}$ shows a maximum as a function of bias or signal frequency [19] :

(a) $$\omega\, \tau_R^{maj} \approx 2.5,$$

(b) $$[G_{p/\omega}]_{max} = \left[\frac{qAN_{is}}{2}\right][2\pi(\sigma_s^2+\sigma_B^2+\sigma_x^2)]^{-1/2} \int_{-2U_B}^{2U_B} \{[\exp(-Z-y_m)]\}$$
$$\{\ln[1+\exp(2y_m)]\}\, dU_s, = K \left[\frac{qAN_{is}}{2}\right]$$

(c) $$y_m = U_s - \bar{U}_s + \ln 2.5, \quad \text{for p-Si}$$

(d) $$y_m = \bar{U}_s - U_s + \ln 2.5, \text{for n-Si}$$

K is a factor whose value generally lies between 0.30 and 0.80. It is to be noted that irrespective of interface state model, $(G_{p/\omega})$ shows a peak if plotted against bias or frequency.

The conductance technique basically consists of calculating C_p and $G_{p/\omega}$ at various frequencies and bias from measured admittance data using Equation (4.23). The next step is to identify the appropriate model(s) for interface states and then accordingly calculate interface state densities, their energy levels and interface state recombination times (and hence capture cross-sections). Clearly the data analysis is quite involved compared to capacitance technique, but the results obtained are quite reliable.

Figure 4.8 represents the conductance-voltage (G-V) characteristics of sample EPOI-7 measured in dark at different value of the signal frequency. Values of the parallel conductance, G_p, and the parallel capacitance, C_p, were calculated from the measured values of the oxide capacitance, C_{ox}, the total MOS conductance, G, and total MOS capacitance C using Equation(4.23). Calculations of G_p and C_p were carried out for all levels of illumination, i.e. zero, L_1, L_2 and L_3. Subsequently, $G_{p/\omega}$ was plotted on a semilogarithmic graph both as a function of bias for different values of frequency, and as a function of frequency for different values of bias. Figure 4.9 diaplays the experimental ln $G_{p/\omega}$ vs V characteristics of sample EPOI-7 for different frequencies corresponding to the dark condition.

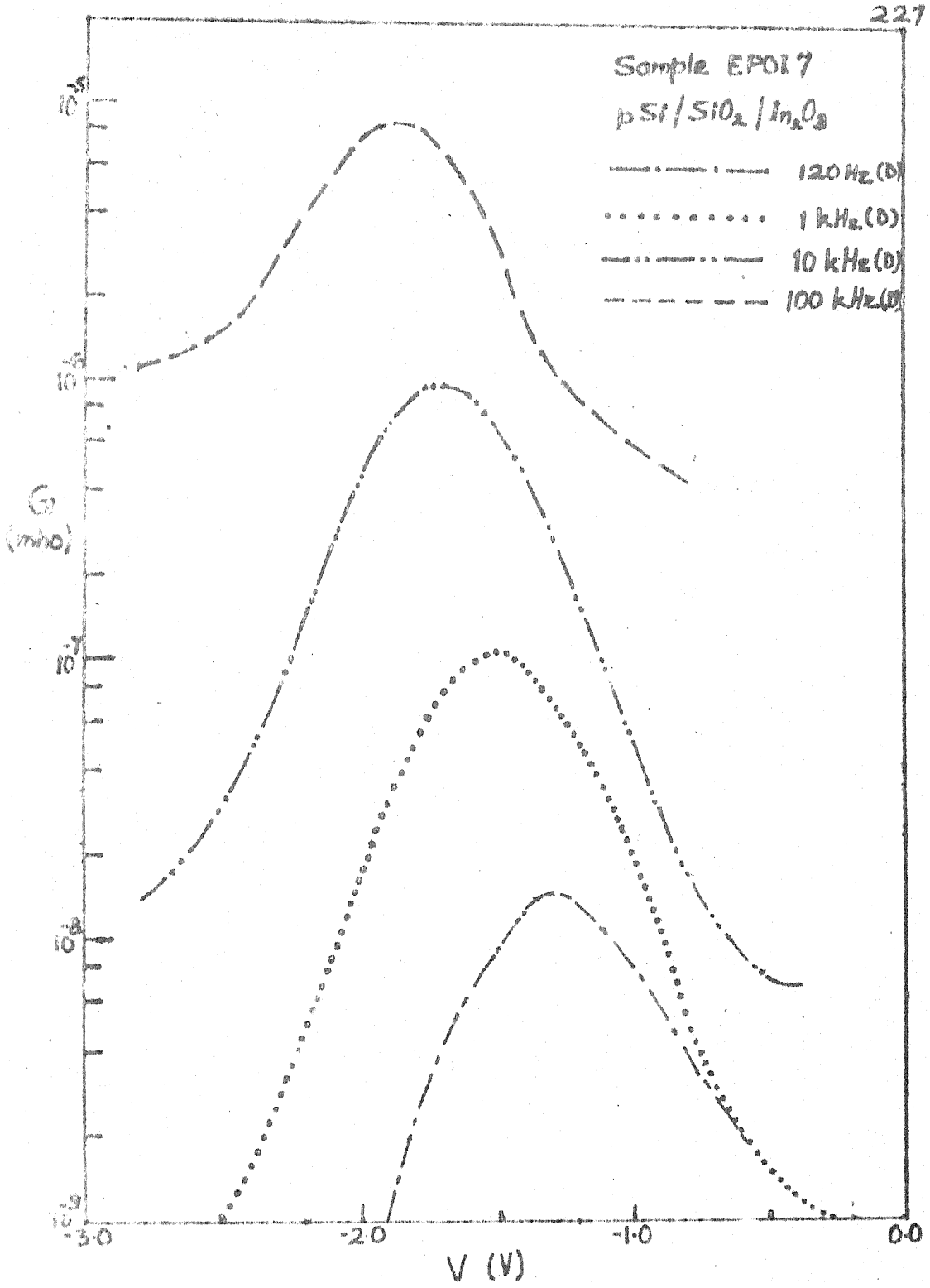


Figure 4.9 Semilogarithmic plot of the conductance vs voltage (G-V) characteristics of sample EPOI-7 measured in dark at different values of the ac signal frequency

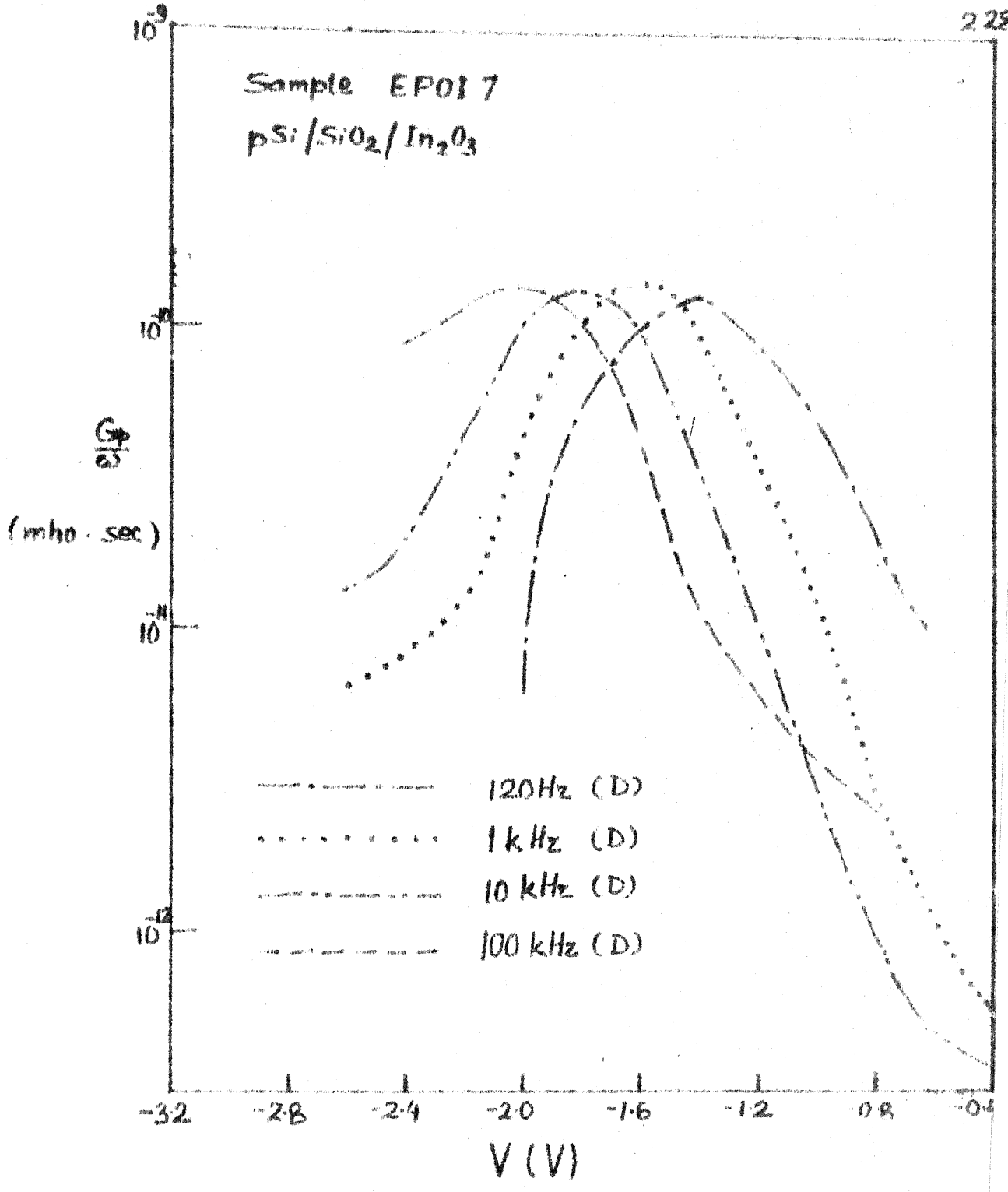


Figure 4.9 Experimental G_p/ω vs V characteristics of sample EPOI-7 at different frequencies obtained from dark admittance measurements

The next step is to identify whether the source of G_p is a single level state, or a continuum of states, or a continuum of states under the influence of statistical fluctuation of the interface potential. To carryout this identification, one has to plot $G_{p/\omega}$ as a function of ω for different values of the bias; and compare the form and the half width of these with the form and the half width of the $G_{p/\omega}$ vs ω characteristics, calculated by Nicollian and Goetzberger for the three cases of single level states, state continuum, and state continuum under statistical fluctuation of Ψ_i [19]. Further processing of the conductance data can proceed in the following manner. If the preceding step reveals that the single level model applies, one can calculate from each ln $G_{p/\omega}$ vs V or each $G_{p/\omega}$ vs ω characteristic showing a peak, the interface state density, N_{is}, and majority carrier time constant, τ_R^{maj}, using Equation (4.25 a , b). On the other hand if continuum of states model, or continuum of states under statistical fluctuation model applies, than Equations(4.27 a , b) and (4.30 a , b) can be used respectively for these models for determining N_{is} and τ_R^{maj}. The energy location E of the interface states, and the majority carrier capture cross-section σ_h for p-type Si (σ_e for n-Si) in dark can be obtained by using following relations :

(a) $E-E_v = q(\phi_p+\Psi_i^{peak})$, for p-Si,

(b) $E-E_v = E_G-q(\phi_n-\Psi_i^{peak})$, for n-Si,

(c) $\sigma_h = \exp(U_s^{peak})/\bar{V}\, N_A\, \tau_R^{maj}$, for p-Si ,

(d) $\sigma_e = \exp(-U_s^{peak})/\bar{V}\, N_D\, \tau_R^{maj}$, for n-Si,

(e) $U_s^{peak} = q\Psi_i^{peak}/kT$

$\bar{V}$ is average thermal velocity of majority carriers, and Ψ_i^{peak} is the interface potential corresponding to the bias at which $(G_{p/\omega})$ has a peak.

Figure 4.10 shows experimental $\ln(G_{p/\omega})$ vs ω characteristics of sample EPOI-7 at various values of the bias and illumination levels. Figure 4.11 reproduces $\ln(G_{p/\omega})$ vs ω for the three different interface state models calculated by Nicollian and Goetzberger [19]. The nature of the dark $G_{p/\omega}$ vs ω characteristics of sample EPOI-7 indicated the statistical model to be the appropriate representation. Values of N_{is} and E in dark, calculated using Equations(4.30 b) and(4.31(a) respectively, for sample EPOI-7 have been plotted in Figure 4.6. The factor K in Equation(4.30 b) can be determined by matching a few N_{is} values obtained in a particular region from conductance and capacitance data. The values of hole capture cross-sections, obtained from Equation(4.31 c), have been presented as a function of interface state energy level in Figure 4.12.

Figure 4.13 displays the conductance vs voltage (G-V) characteristics of sample EPOI-7 measured at different frequencies under illumination level L_1. Figure 4.14 displays the

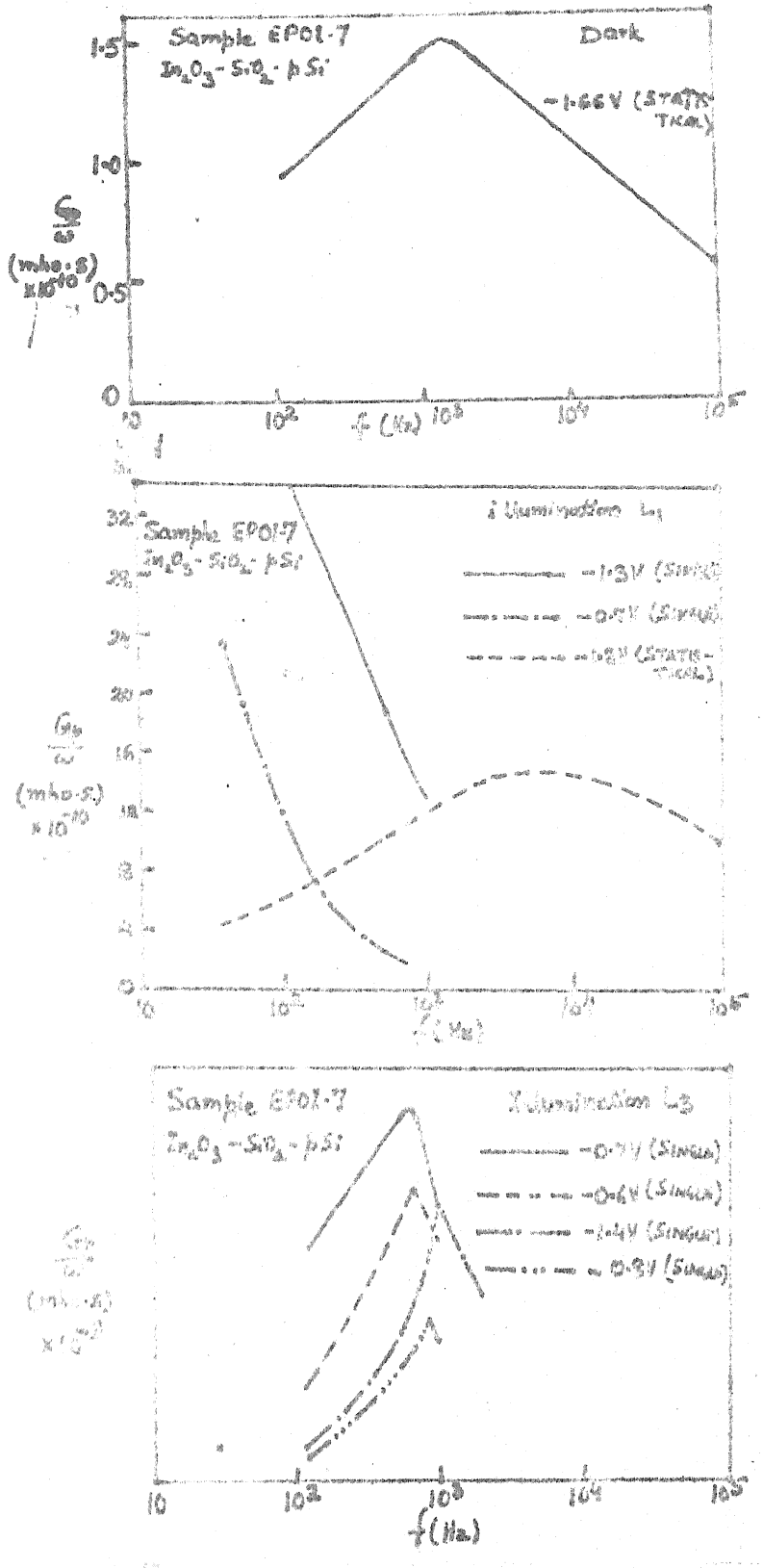


Figure 4.20 Experimental G_p/ω vs ω characteristics of sample EPOI-7 at various values of the bias and illumi-

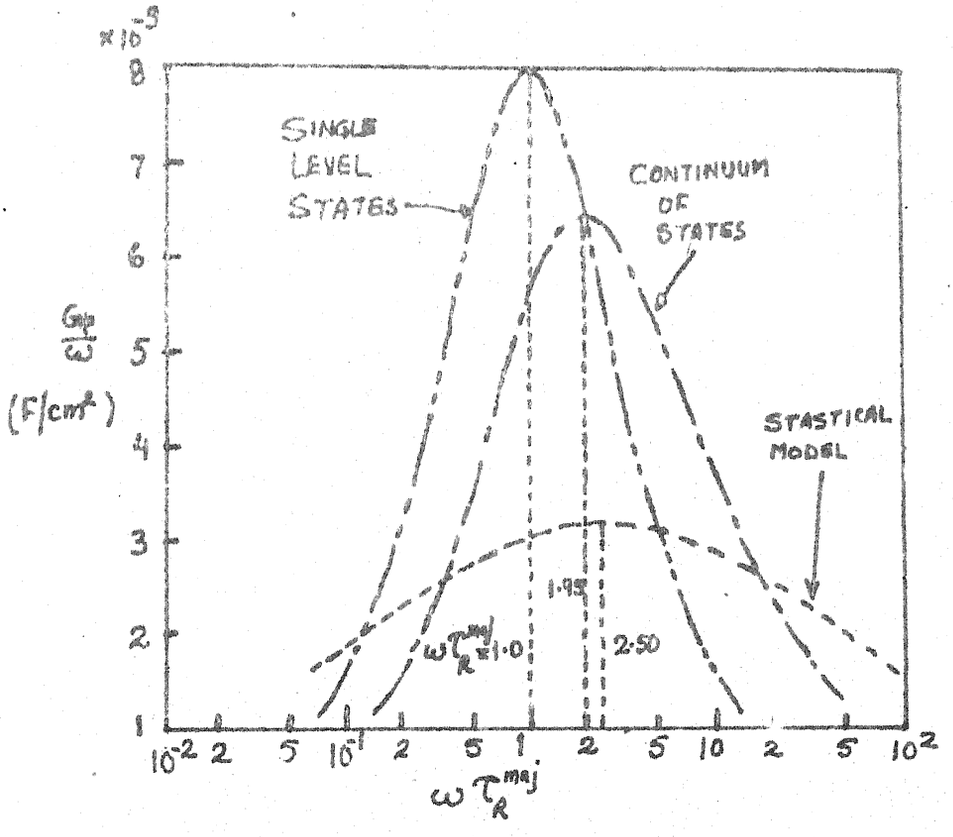


Figure 4.11 Theoretical G_p/ω vs ω for the cases of single level states, state continuum, and state continuum under statistical fluctuation of Ψ_i, as calculated by Nicollian and Goetzberger [19]

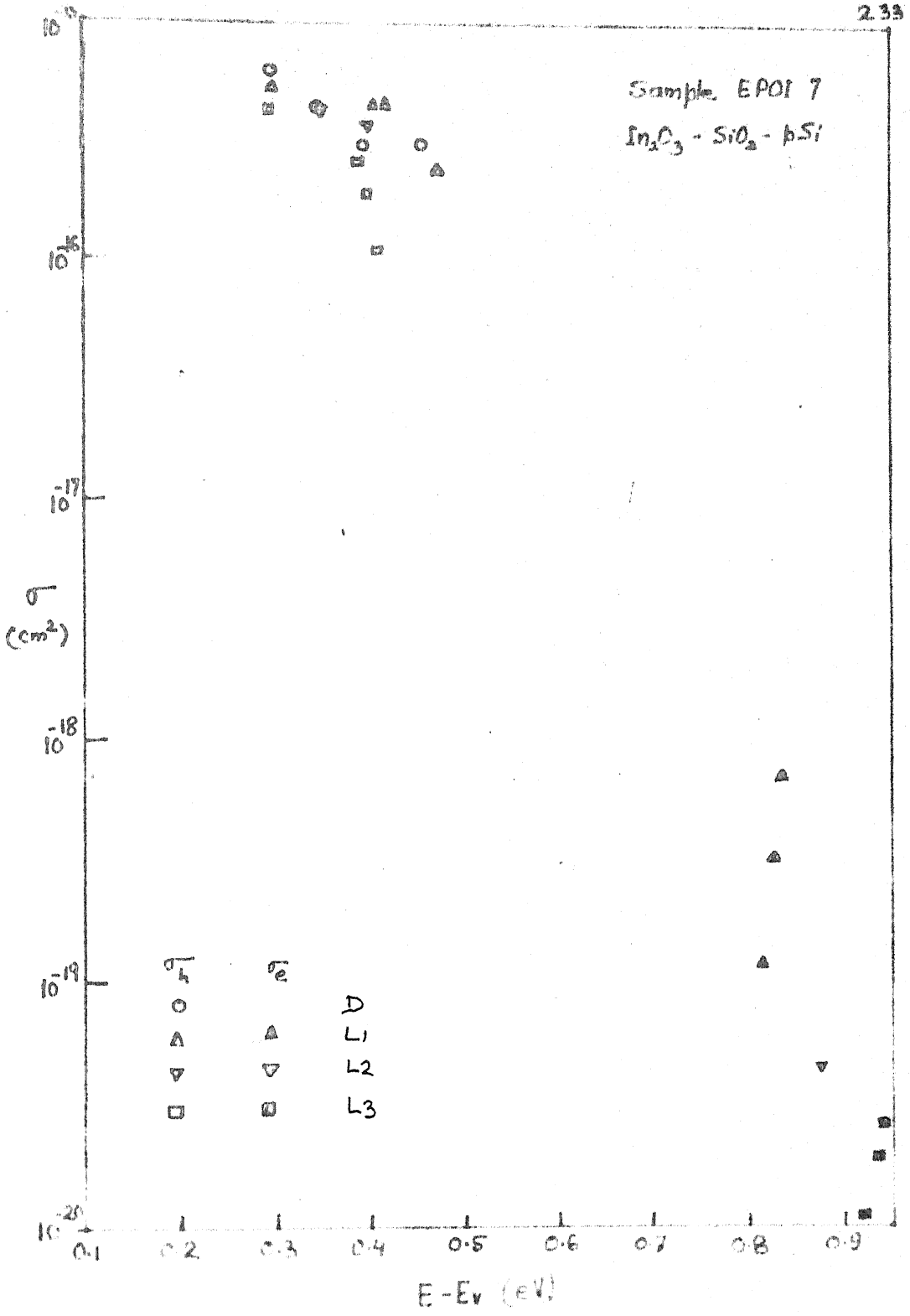


Figure 4.12 Experimental interface capture cross-section for holes, σ_h, and for electrons, σ_e, vs band gap energy of the states of sample EP01-7 obtained from conductance data measured under illumination levels of zero, L_1, L_2, and L_3

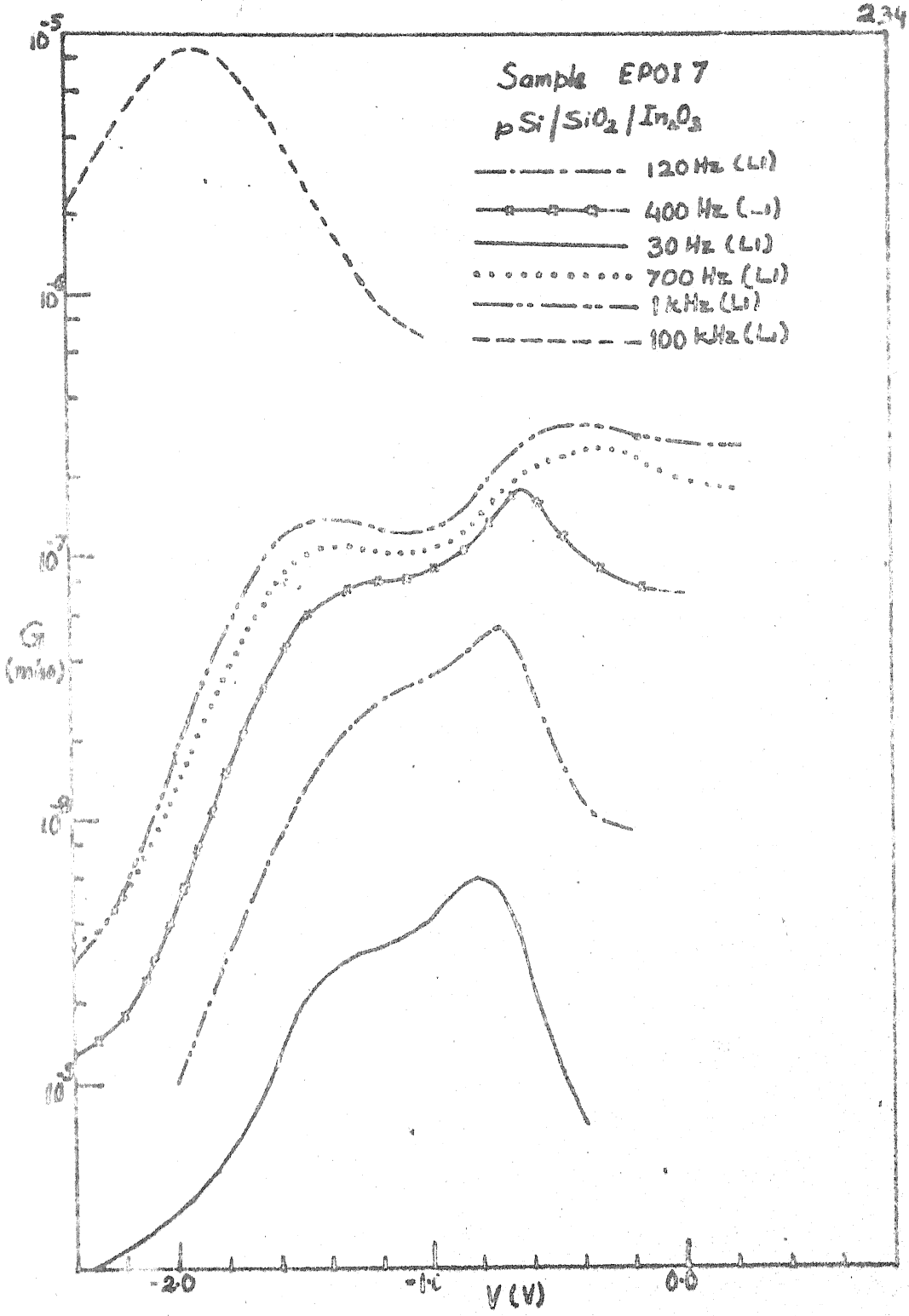


Figure 4.18 Semilogarithmic plots of conductance vs voltage (G-V) characteristics of sample EPOI-7 measured at different frequencies under illumination level L_1

experimental ln $(G_{p/\omega})$ vs V characteristics of sample EPOI-7 obtained under illumination level L_1 at different frequencies. Nicollian and Goetzberger [19] have argued that, under the dark condition, charge exchange between the interface state and the majority carrier band is likely to prevail even in the inversion region. In contrast, under illumination, charge exchange can take place either between the conduction band and interface states at the electron quasi-Fermi level, or between the valence band and interface states at the hole quasi-Fermi level. The former will prevail if $\sigma_e.n_s > \sigma_h p_s$, otherwise, the latter. Since values of the capture cross-sections have, firstly, to be determined from $G_{p/\omega}$ data, it would facilitate data analysis, if there was another way of ascertaining the source of a particular set of $G_{p/\omega}$ characteristics. This could be done easily if capture cross-sections were independent or weak functions of the band gap energy. In that case, if hole exchange with the valence band was dominant, $(G_{p/\omega})_{max}$ would move towards more positive values of Ψ_i with decreasing frequency, and vice-versa if electron exchange with the conduction band was involved. If the capture cross-sections vary strongly with band gap energy, the above procedure may not provide clear clue.

The experimental ln $(G_{p/\omega})$ vs V characteristics under light of Figure 4.14, display two sets of peaks; one set generated by hole exchange between the valence band and interface states at the hole quasi-Fermi level; the other set generated by exchange

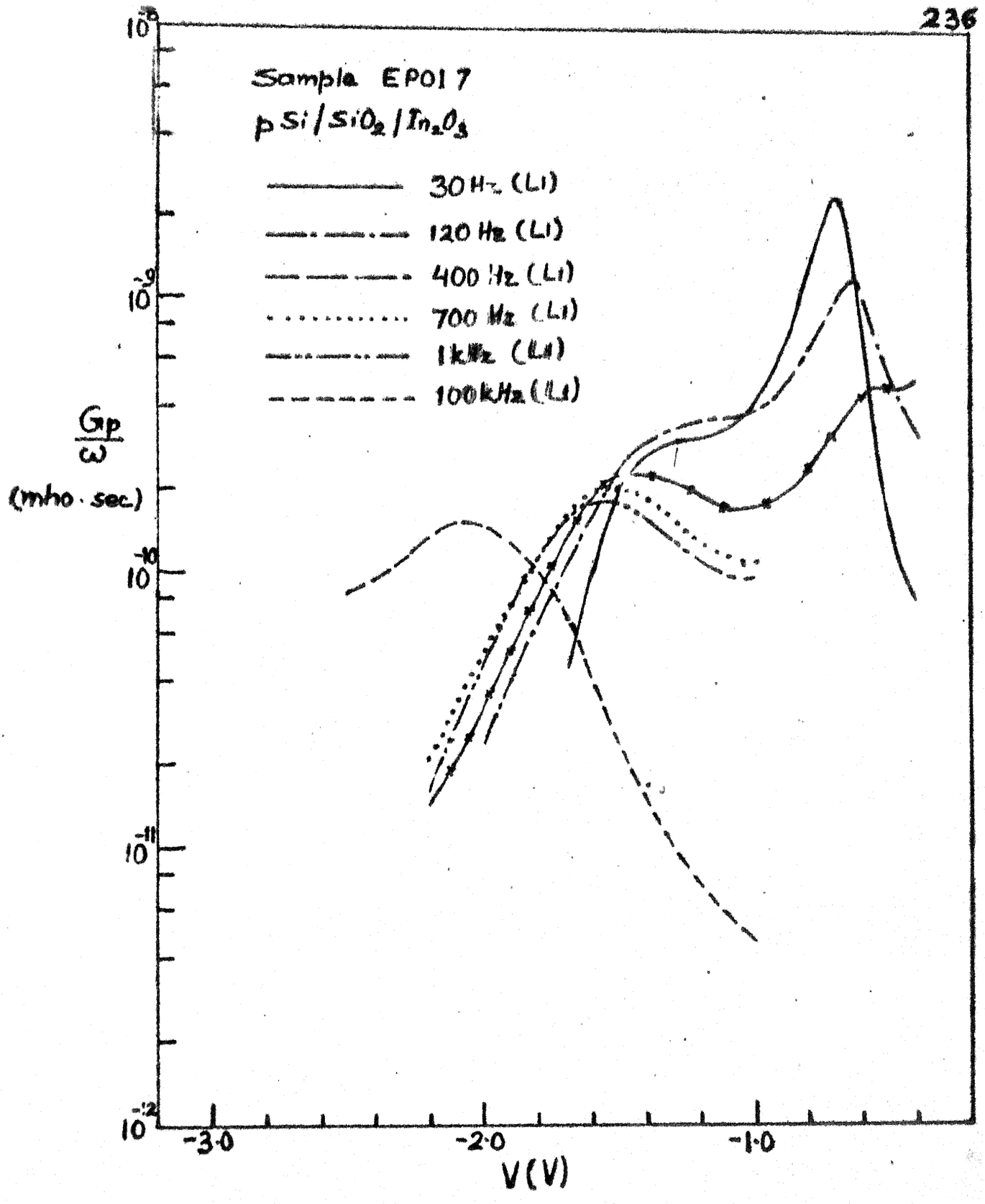


Figure 4.14 Experimental G_p/ω vs V characteristics of sample EP01-7 obtained under illumination level L_1 at different frequencies

of electrons between the conduction band and interface states located at the electron quasi-Fermi level. For the former set, values of Ψ_i corresponding to $(G_{p/\omega})_{max}$ are in the depletion regime, and the same for the latter are in the weak inversion regime, cf. Figure 4.5. Identification of which type of carriers are involved in charge exchange, for each of the two sets of peaks in Figure 4.14, did not present any difficulties, except that in case of the 30 Hz and 120 Hz characteristics, there is considerable overlap between $G_{p/\omega}$ values, contributed by the two sources, resulting in broad shoulders.

$G_{p/\omega}$ vs ω characteristics plotted in Figure 4.10, belonging to each of the sets of characteristics of Figure 4.14 indicated that the statistical single model applied to the set generated by hole exchange and single level model applied to the set generated by electron exchange. Accordingly, values of N_{is}, E, σ_h and σ_e were evaluated under illumination from $(G_{p/\omega})_{max}$ data of Figure 4.14 using the relations of Equations (4.25 a), (4.25 b), (4.30 a), (4.30 b), (4.31 a), (4.31 c), and the following expressions, for the condition when electron imref became dominant under illumination.

(a) $E-E_v = q(\phi_p + \Psi_i^{peak}) + \delta E_F$, for p-Si, electron exchange,

(b) $\sigma_e = \exp(U_s^{peak} - \delta E_F)/\sqrt{V}\, N_A\, \tau_R^{min}$, for p-Si, electron exchange,

(c) $\omega\, \tau_R^{min} = 1.0$, for single level state, electron exchange in p-Si , (4.32)

The values of N_{is}, E, σ_h and σ_e corresponding to illumination intensity L_1 have been presented in Figures 4.6 and 4.12. In a manner similar to that for illumination intensity L_1, $G_{p/\omega}$ data obtained under illumination level L_2 and L_3 were processed. For both these levels, two sets of $G_{p/\omega}$ peaks were obtained, one set arising out of hole exchange and following statistical/single model, the other set arising out of electron exchange and following the single level model. Experimental values of state density, their energy location, hole and electron capture cross-sections, obtained for illumination intensities L_2 and L_3 have been plotted in Figures 4.6 and 4.12.

4.4 RESULTS AND DISCUSSION

4.4.1 Spray Deposited TCOS Structures

Figure 4.15 presents a selection of capacitance vs voltage (C-V) characteristics of a spray hydrolysis deposited Sn doped In_2O_3-SiO_2-nSi device, sample SNOI-3, measured at different frequencies, and in dark and under illumination. It can be seen that under optical illumination, the device capacitance saturated to the silicon oxide capacitance both in strong accumulation and in strong inversion. The silicon oxide thickness, t_{ox}, was calculated to be 146 Å from the value of the oxide capacitance, assuming a dielectric constant of 3.82 for SiO_2 layer. At frequencies above 50 kHz, the device capacitance exhibited dispersion in strong accumulation due to

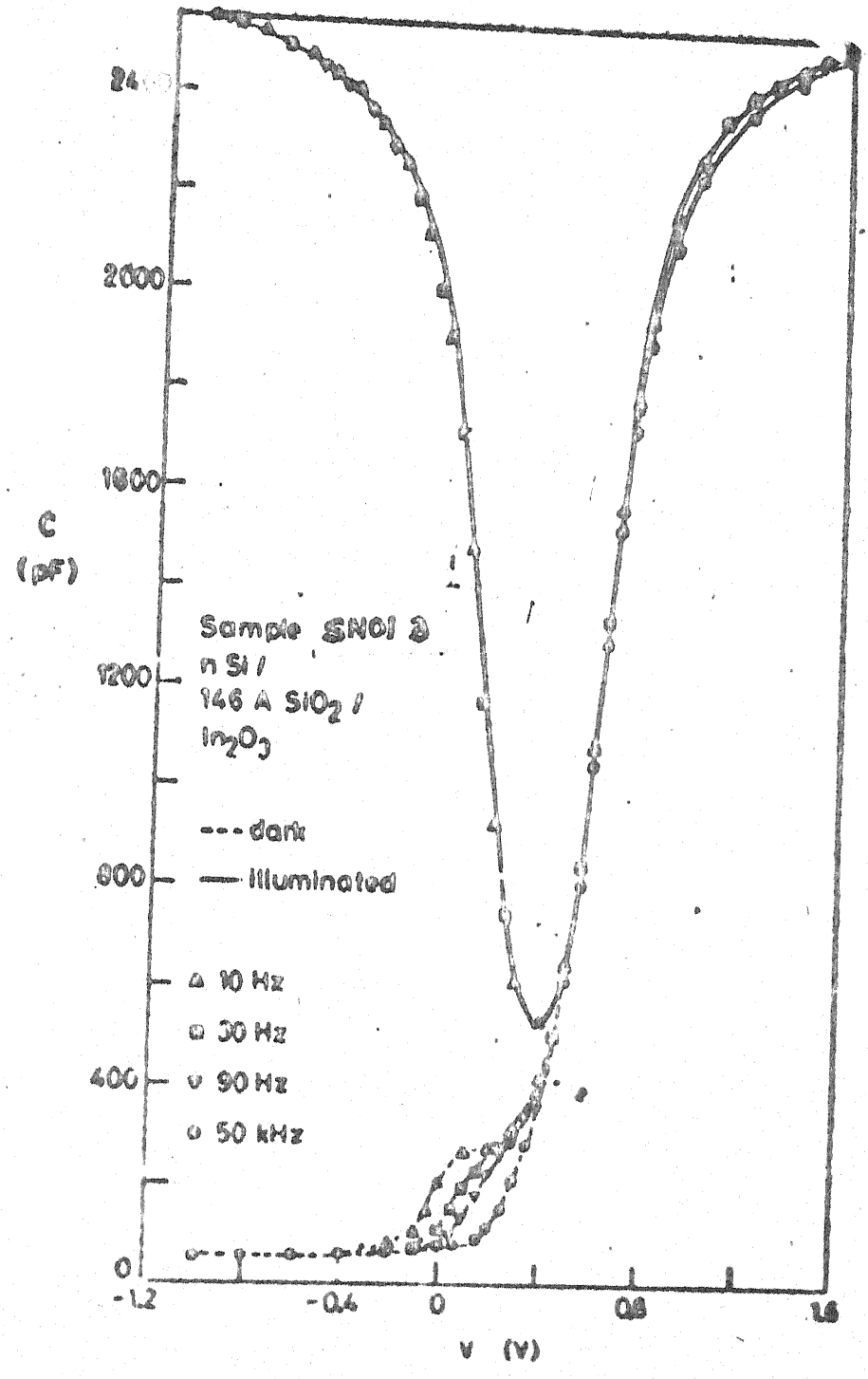


Figure 4.15 A selection of capacitance vs voltage (C–V) characteristics of a spray hydrolysis deposited Sn doped In_2O_3–SiO_2–nSi device, sample SNOI-3, measured at different frequencies, and in dark and under illumination

a high series resistance. The high series resistance may have resulted from the high bulk silicon resistivity of about 10 Ohm-cm. The doping density, N_D, was calculated from the constant high frequency capacitance in strong inversion in dark. This came out to be 2.4×10^{14} cm^{-3} and the corresponding bulk Fermi potential, ϕ_n, was calculated to be 0.30 V.

The C-V characteristics of Figure 4.15 indicate that, at 10 Hz, the inversion layer does not respond to the ac signal in dark. Also the interface states in the minority carrier band gap half are not able to follow the 10 Hz are signal in the dark. The situation is drastically changed under illumination. No dispersion can be observed between the 90,30 and 10 Hz characteristics under illumination, and hence the 10 Hz characteristic obtained under illumination, may be considered to be the low frequency equilibrium capacitance. The 10 Hz C-V characteristic under illumination was graphically integrated to determine Ψ_i vs V relationship under illumination, and was used for determining interface state density distribution under illumination. The 10 Hz C-V characteristic in the dark, for voltages higher than 0.20 V, was also made use of to calculate interface state density distribution and to determine Ψ_i vs V relationship in dark.

The capacitance data analysis was carried out as discussed in Section 4.3.1. Figure 4.16 contains experimental low frequency equivalent parallel capacitances C^p_{lfd} in dark, and C^p_{lfl}

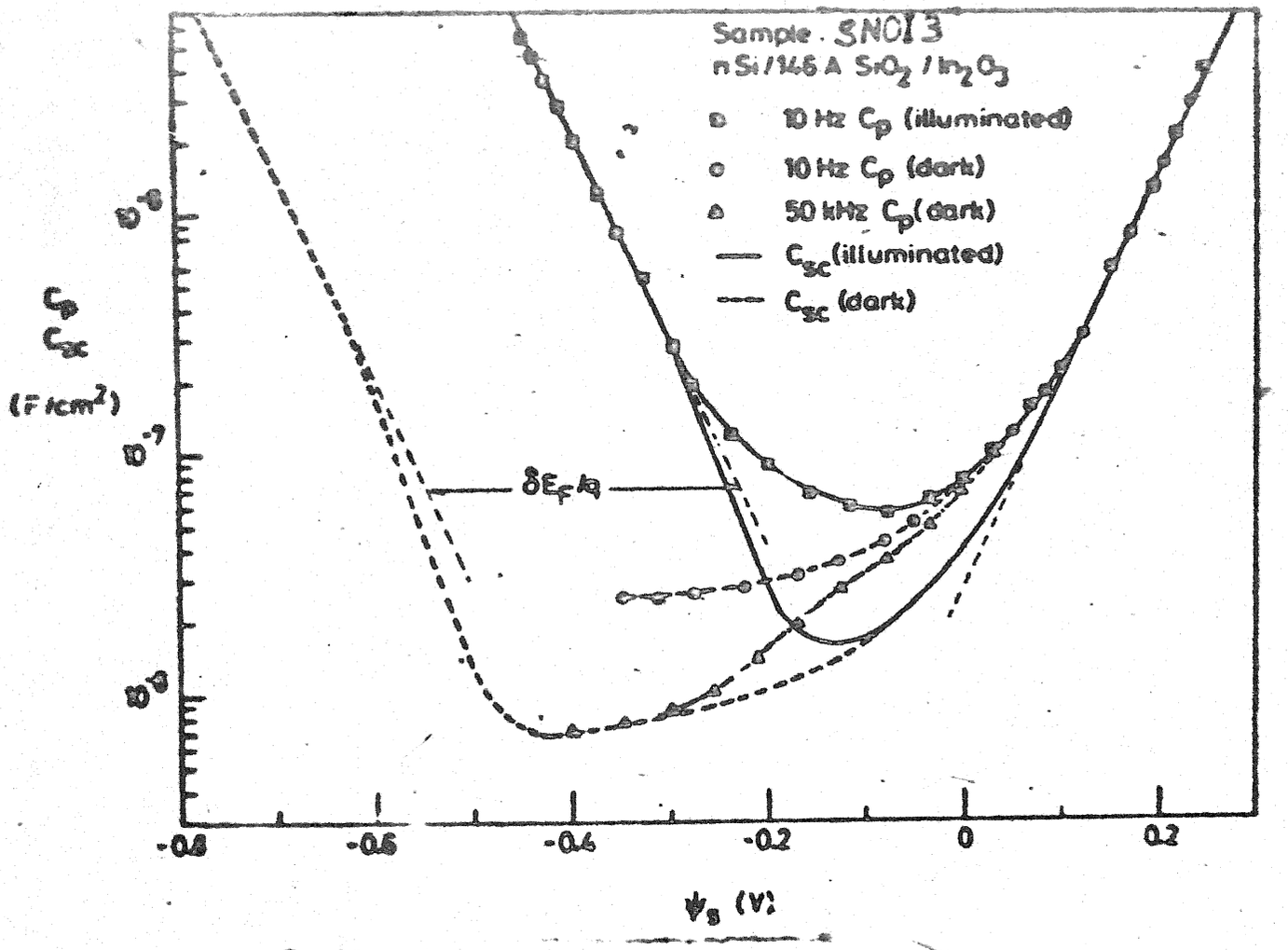


Figure 4.16 Semilogarithmic plot of experimental C_{lf}^{p} vs ψ_i and calculated C_{sc} vs ψ_i characteristics of sample SNOI-3, in dark and under illumination

under light, and calculated space charge capacitances C_{scd} in dark and C_{scl} under illumination, for sample SNOI-3, as a function of interface potential Ψ_i. Figure 4.16 also includes 50 kHz equivalent parallel capacitance C^p_{hfd} vs Ψ_i characteristic in dark, which indicates that even at 50 kHz, a considerable amount of interface states contributed to the parallel capacitance in dark around flat band, however, in inversion and around midband, the high frequency parallel capacitance curve matches well with the calculated space charge capacitance curve. The illuminated 10 Hz parallel capacitance under illumination is found to match well with calculated space charge capacitance under illumination in strong inversion. Also, the low and high frequency parallel and space charge capacitance curves in dark and under illumination matched very well in strong accumulation. Consequently, the integration constant for graphical integration of low frequency C-V curve, and quasi-Fermi level separation could be easily determined. The quasi-Fermi level separation determined from parallel shift of illuminated ln C_{scl} vs Ψ_i curve compared to dark ln C_{scd} vs Ψ_i curve in strong inversion came out to be 0.32 eV.

Probably because of high series resistance, $G_{p/\omega}$ vs V or ω characteristics were not suitable for further processing, hence, the capture cross-sections could not be determined experimentally for this sample. Under illumination, the issue of hole vs electron exchange with states was resolved as discussed in Sec.4.3.1

by determining location of quasi-Fermi levels with respect to mid gap, by taking into consideration the location of states contributing to the observed peak in N_{is}, and by omitting the interface potential region of uncertainity in dominant imref.

The interface state density distribution for sample SNOI-3, calculated from C_{lf}^{p} and C_{sc} vs Ψ_i characteristics of Figure 4.16, as a function of band gap energy is depicted in Figure 4.17. Interface state densities of sample SNOI-3 obtained from dark and illuminated capacitance data nicely augment each other to form a section of U shaped profile which is generally observed in thermally grown SiO_2-Si system. The interface state density around mid gap was found to be about $1x10^{11}$ cm^{-2} V^{-1}. The illuminated capacitance data of sample SNOI-3 revealed a peak in N_{is} located at about 0.30 eV above valence band arising due to hole exchange between valence band and hole imref. The density of interface states at the peak was about $4.0x10^{11}$ cm^{-2} V^{-1}. Since dark capacitance data could not provide any information about interface state density in lower half of the band-gap in case of sample SNOI-3, it could not be ascertained if this peak was observed under dark condition also, or was due to interaction with light.

Figure 4.18 displays a selection of capacitance vs voltage characteristics of a spray hydrolysis deposited In_2O_3-SiO_2-pSi device, sample SPOI-1, measured at different frequencies, and in

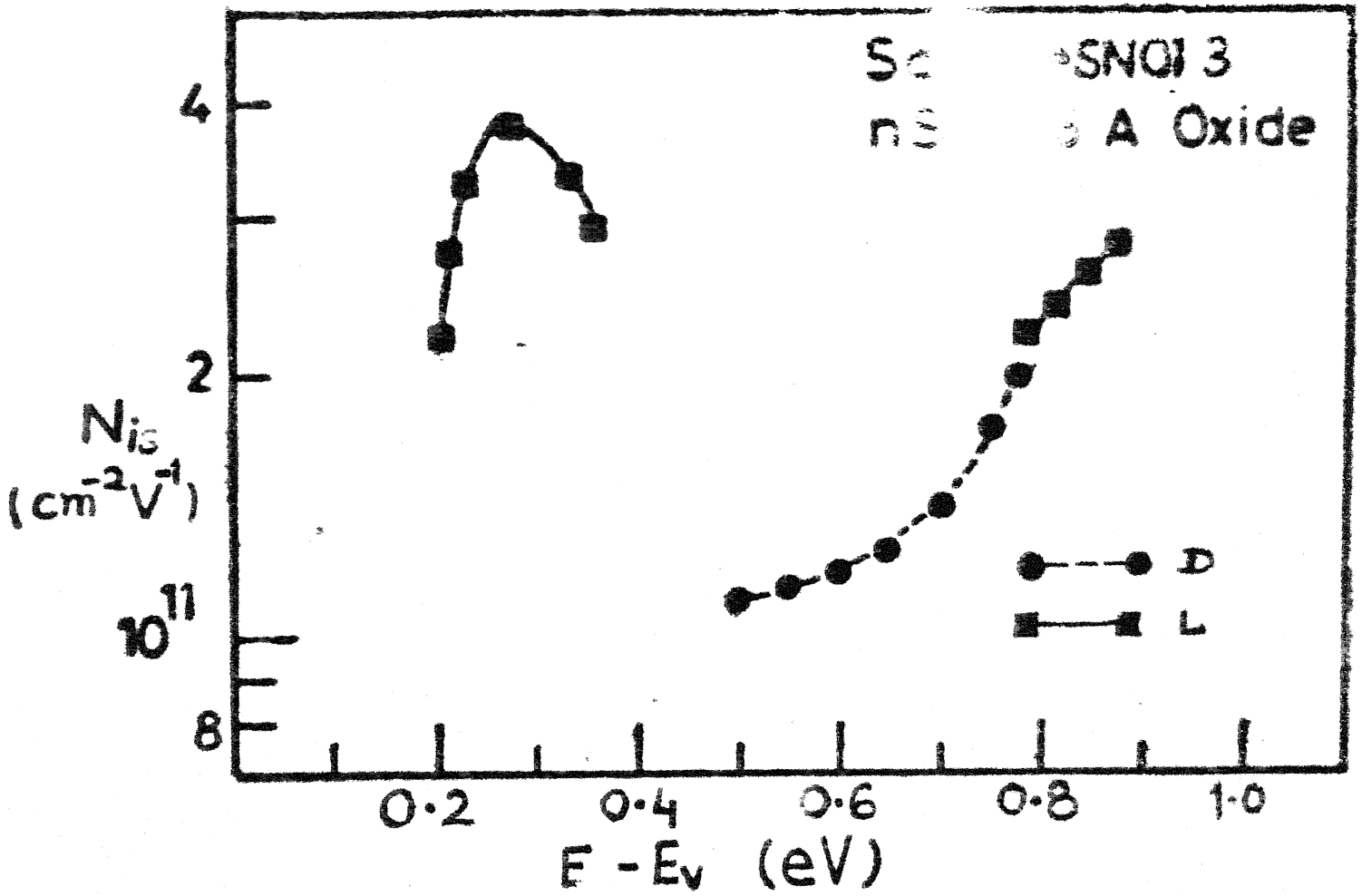


Figure 4.17 Experimental interface state density, N_{is}, as a function of band gap energy, E, for sample SNOI-3 obtained from the dark and from illuminated capacitance-voltage characteristics

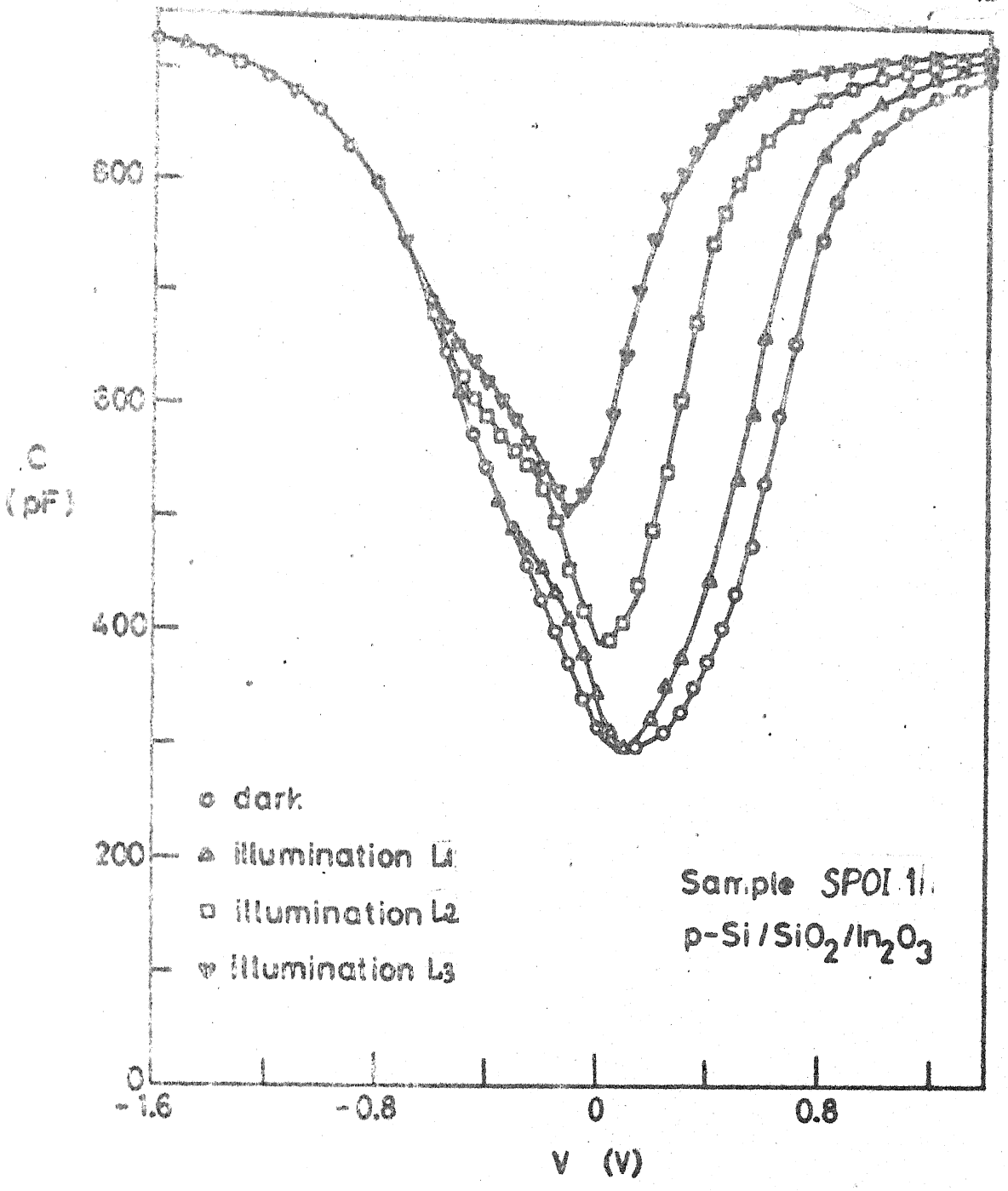


Figure 4.18 A selection of capacitance vs voltage (C-V) characteristics of a spray hydrolysis deposited Sn doped In_2O_3-SiO_2-pSi device, sample SPOI-1, measured at different frequencies, and in dark and under illumination levels L_1, L_2, and L_3

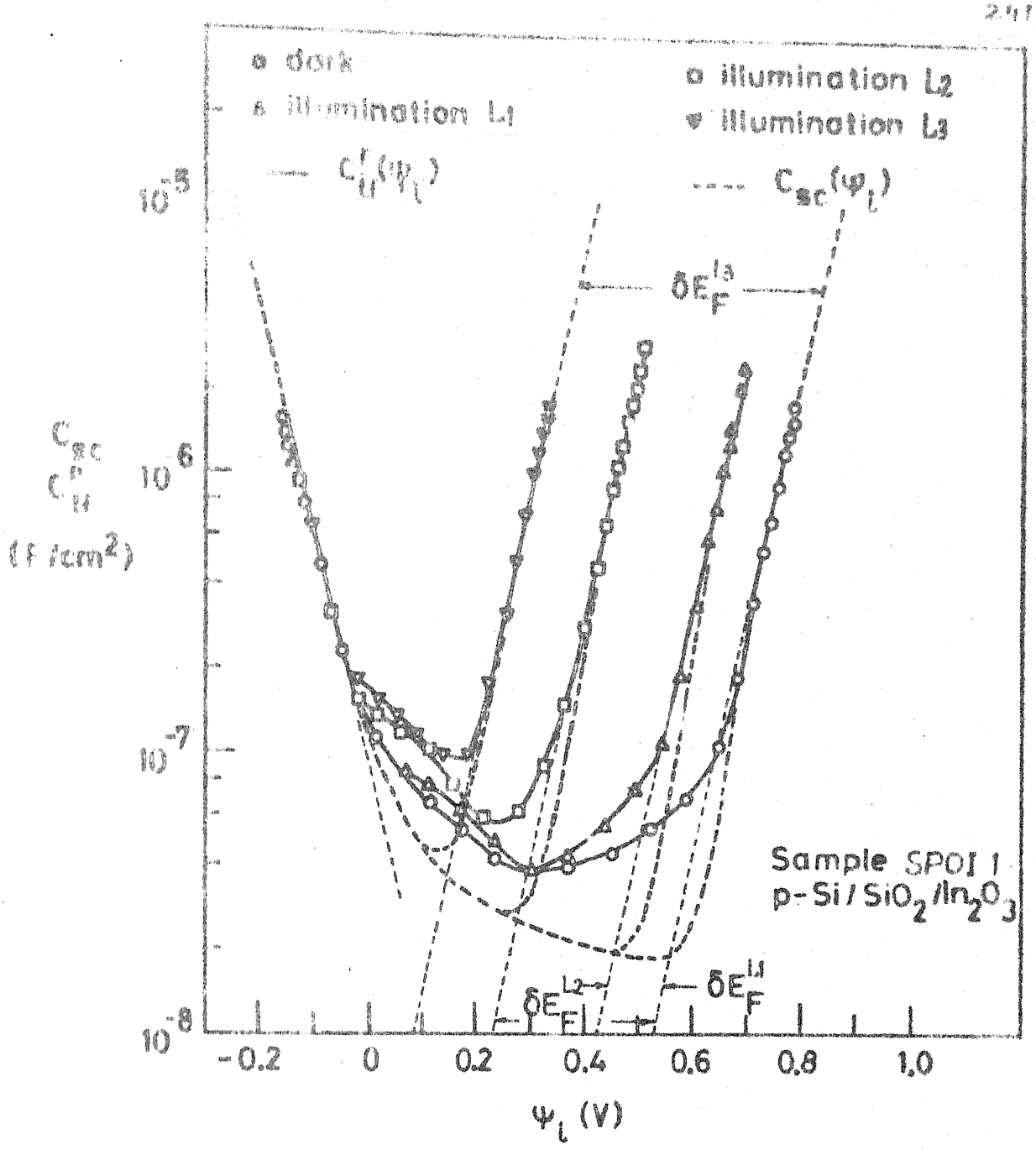


Figure 4.19 Semilogarithmic plot of experimental C_{if}^{p} vs ψ_i and calculated C_{sc} vs ψ_i characteristics of sample SPOI-1 in dark and under illumination levels L_1, L_2, and L_3

L_1,L_2 and L_3 were obtained as 0.10 eV, 0.30 eV, and 0.45 eV respectively. Using the experimentally obtained value of imref separation, δE_F, for each illumination level, space charge capacitance under illumination, C_{scl}, vs interface potential, Ψ_i, curves were calculated and plotted in Figure 4.19.

The interface state density distribution, for sample SPOI-1, in dark, calculated from difference in C^p_{lfd} and C_{scd}, has been plotted as a function of band gaps energy in Figure 4.20. In case of sample SPOI-1 also, the issue of hole vs electron exchange with states under illumination was resolved as discussed in Section 4.3.1. The conductance technique could not be used for determining capture cross-sections of states due to high series resistance of sample SPOI-1. After the dominant imref was determined, corresponding energy location of the interface state densities calculated were determined. The regions near the band-edges were avoided for N_{is} determination as inaccuracies in the magnitude of N_{is} could be considerable. Interface state density distributions obtained for illumination levels L_1,L_2, and L_3 for sample SPOI-1, are also presented in Figure 4.20.

The interface state profile obtained from dark capacitance data shows the usual U shape profile in the band energy region of 0.15 to 0.85 eV above valence band with mid gap interface state density of about $1x10^{11}$ cm^{-2} eV^{-1} (cf. Figure 4.20). This

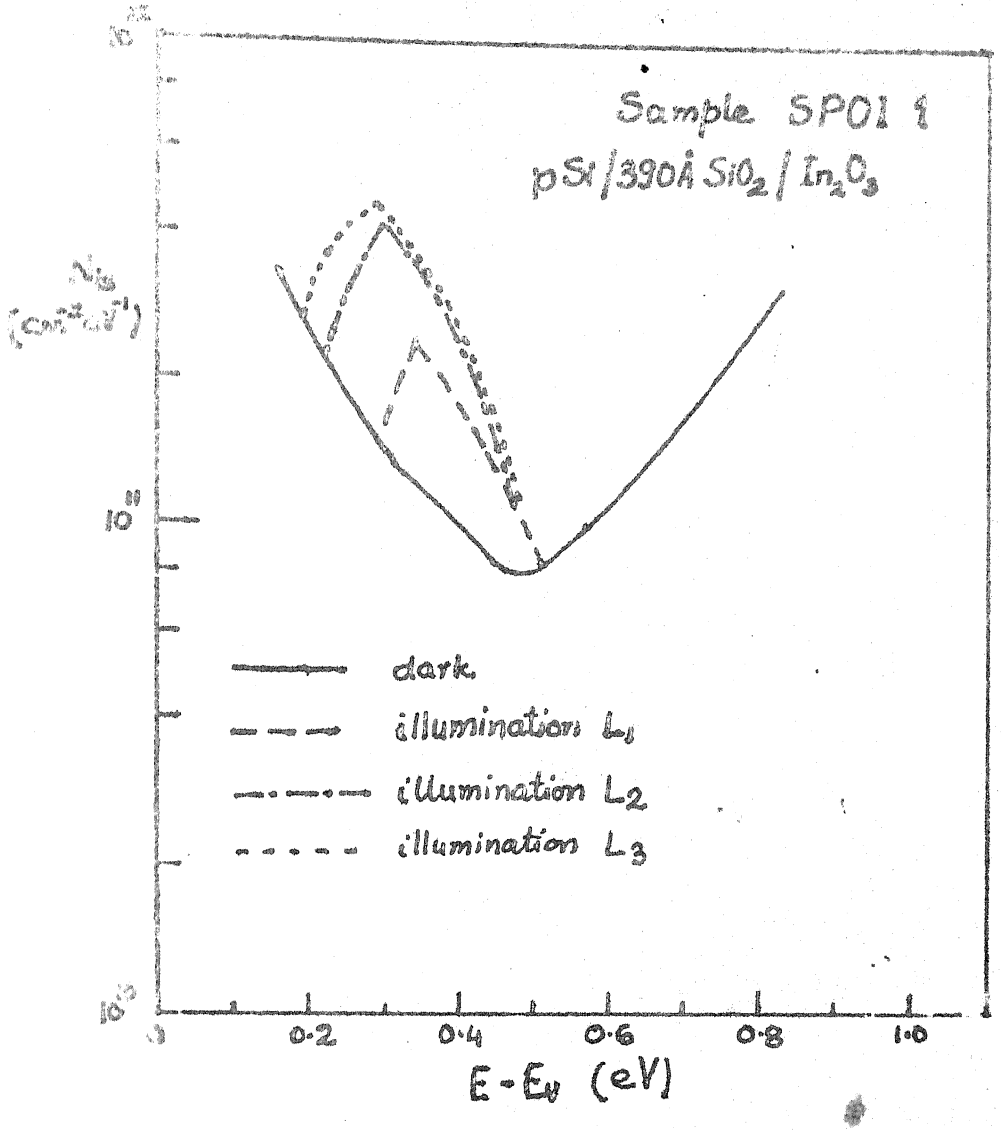


Figure 4.20 Experimental interface state density, N_{is}, as a function of band gap energy, E, for sample SPOI-1 obtained from the capacitance-voltage characteristics in dark and under illumination levels L_1, L_2, and L_3

U shape profile obtained in dark is similar to that observed in case of sample SNOI-3 (cf. Figure 4.17) in upper half band-gap. However, contrary to sample SNOI-3, the state density profile in the lower half band gap could be determined from dark C-V data of sample SPOI-1. Though the state density profile in lower half band gap does not indicate any peak in dark, it shows slight hump around 0.30-0.50eV above valence band. Under illumination, the state density profile matches with dark state density profile in upper half band gap. However, illumination level L_1 reveals a distinct interface state density peak around 0.34 eV above valence band with peak state density of about 2.4×10^{11} cm^{-2} V^{-1}. As the illumination level increases, the magnitude of the peak increases from 2.4×10^{11} to 4.6×10^{11} cm^{-2} V^{-1}, and its location shifts towards valence band edge from 0.34 eV - 0.29 eV. It may be noted that both the samples SNOI-3 and SPOI-1 showed peaks under illumination with about the same peak interface state density and the location around 0.30-0.35 V above valence band. Increase in peak magnitude and shift in its location with illumination level suggests that there are optically assisted states in this region, though in other regions the illumination did not change state density profile. The magnitude of interface state density peak under illumination appears to be saturating with increase in illumination level.

4.4.2 Chemical Vapor Deposited TCOS Structures

Interface state investigation in chemical vapor deposited TCOS structures was also carried out by the capacitance technique, as due to high sheet resistance of SnO_2 films, clear G_p/ω peaks could not be obtained. As in case of spray deposited TCOS structures, capture cross-sections for the majority and minority carriers could not be determined for chemical vapor deposited samples, and the dominant imref was identified as discussed earlier for such cases.

Figure 4.21 displays capacitance vs voltage characteristics of a typical chemical vapor deposited undoped SnO_2-SiO_2-nSi device, sample CNOT 51, obtained at 30 Hz in dark and under illumination. Though inversion layer and interface states in the minority carrier band gap half could not follow the 30 Hz ac signal in dark, under illumination they followed the ac signal. The 30 Hz C-V characteristic under light can be considered as the low frequency equilibrium frequency since no dispersion was observed between the 30 Hz and 120 Hz characteristics under illumination. It could be seen that the 10 kHz C-V characteristic in dark could not attain oxide capacitance in strong accumulation indicating a high series resistance of the sample CNOT 51. The silicon oxide thickness was calculated to be 450 Å from the value of oxide capacitance. The bulk doping density N_D was found to be 5.0×10^{15} cm^{-3} and the

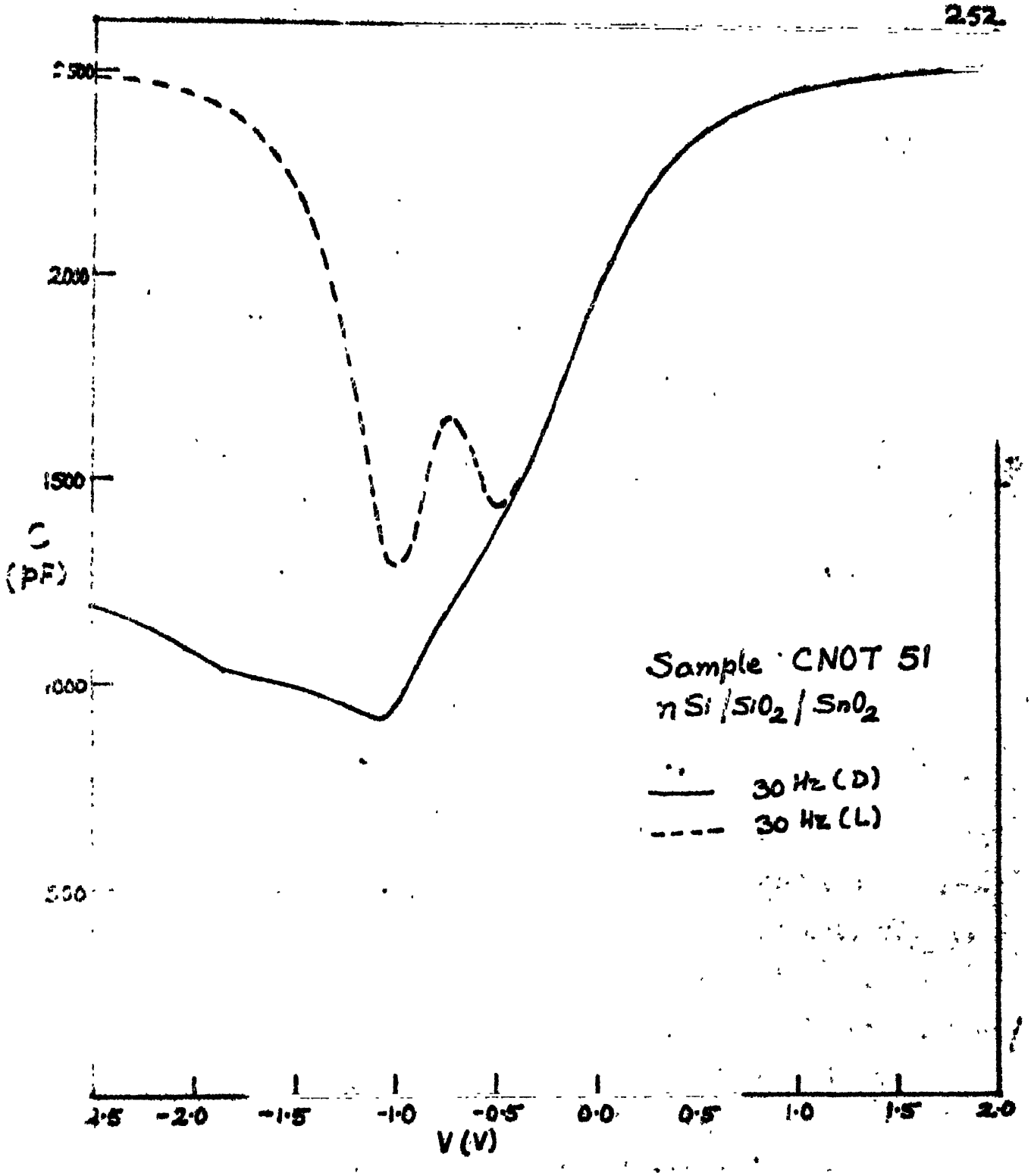


Figure 4.21 Low frequency (30 Hz) capacitance vs voltage characteristics of a typical chemical vapor deposited undoped SnO_2-SiO_2-nSi device, sample CNOT-51, in dark and under illumination

corresponding bulk Fermi potential, ϕ_n, was 0.23 V. Low frequency (30 Hz) illuminated C-V curve was graphically integrated to determine Ψ_i vs V relationship.

Figure 4.22 displays calculated space charge capacitance in dark, C_{scd}, vs Ψ_i characteristic on a semilogarithmic scale. Experimentally obtained low frequency parallel capacitance under light, C^p_{lfl} is also plotted in Figure 4.22 and the parallel shift in ln C^p_{lfl} plot in strong inversion resulted in quasi-Fermi level separation of 0.21 eV. Using this value of quasi-Fermi level separation, space charge capacitance under light C_{scl}, was calculated and plotted in Figure 4.22. C_{scd}, C_{scl} and C^p_{lfl} showed good matching in strong accumulation and C_{scl} and C^p_{lfl} showed good matching in strong inversion. The interface state density distribution under illumination was calculated from C^p_{lfl} and C_{scl} values at each interface potential.

Figure 4.22 displays a peak near valence band edge in low-frequency equivalent parallel capacitance under light, C^p_{lfl} vs interface potential, Ψ_i, curve. This peaked distribution is due to charge exchange between valence band and hole imref. The corresponding interface state density distribution obtained under illumination is displayed in Figure 4.23. As in case of both the spray deposited samples SPOI 1 and SNOI 3, the chemical vapor deposited sample CNOT 51 also shows an N_{is} peak under

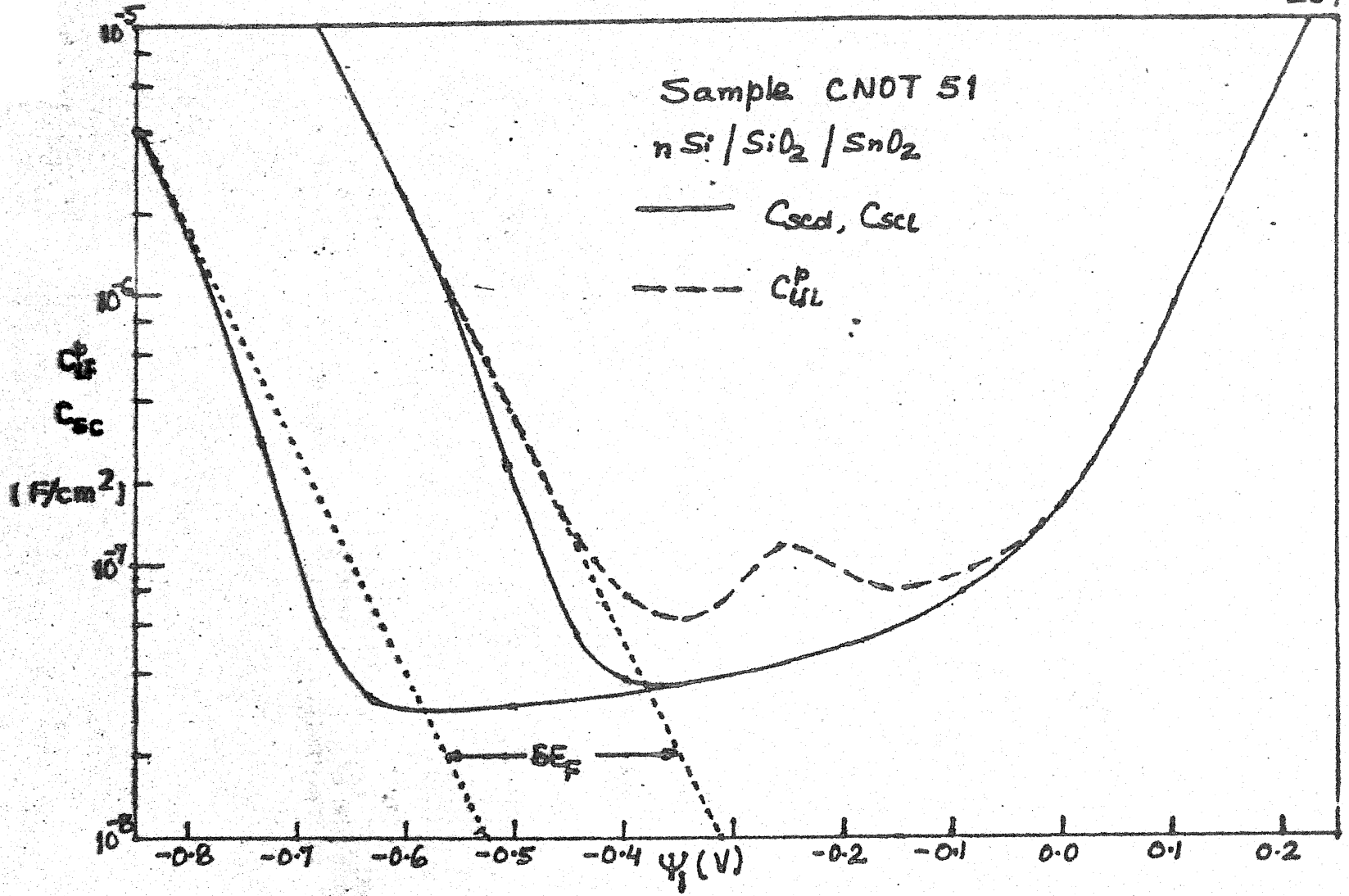


Figure 4.22 Semilogarithmic plot of experimental C'_{ir} vs ψ_i characteristic under illumination and calculated C_{sc} vs ψ_i characteristics of sample CNOT-51 in dark and under illumination

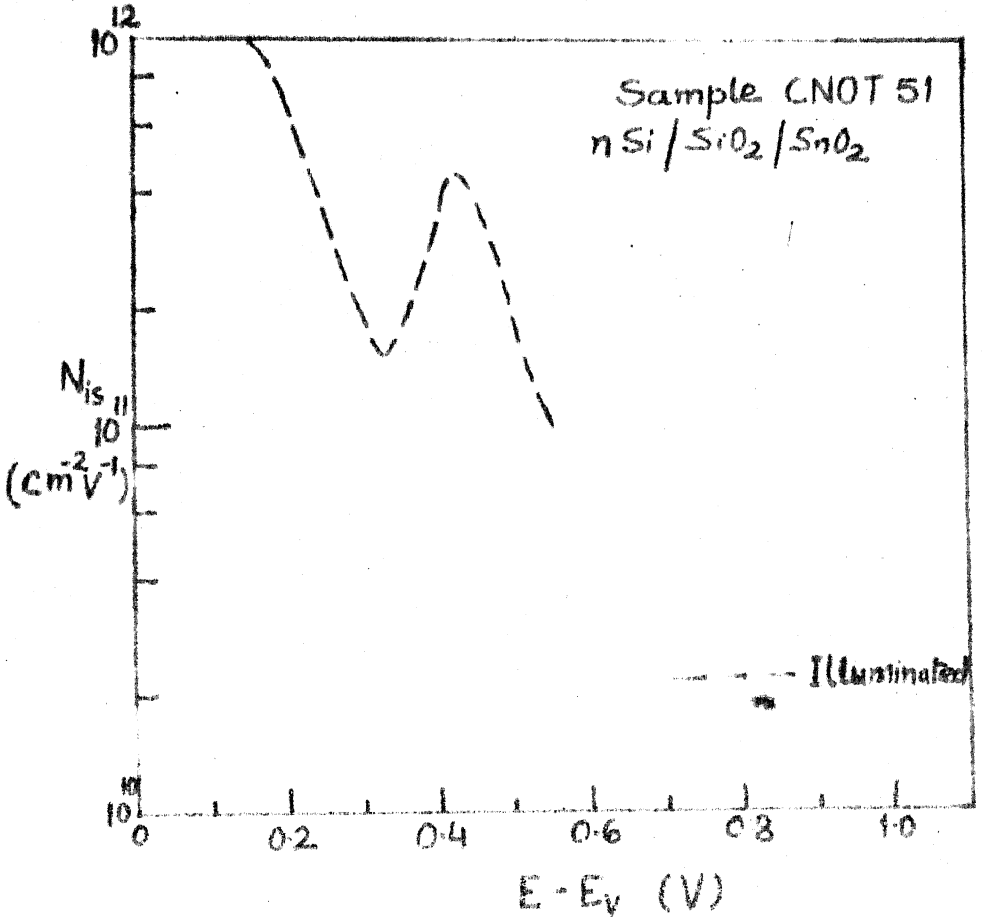


Figure 4.23 Experimental interface state density, N_{is}, vs band-gap energy, E, profile for sample CNOT-51 obtained from the C-V characteristic under illumination

illumination located at about 0.42 eV above valence band with the peak magnitude of 4.6×10^{11} states/cm^2/ V. However, in the absence of interface state data in dark, it could not be ascertained if such a peak was due to illumination or the dark $N_{is}(E)$ also had a peak.

Figure 4.24 presents a selection of capacitance vs voltage characteristics of a typical chemical vapor deposited Sb doped SnO_2-SiC_2-Si device, sample CNOT 47, measured at different frequencies, and in dark and under illumination levels L_1, L_2, L_3. It is to be noted that $L_1 < L_2 < L_3$ and that these levels were not same for different samples. The 30 Hz dark C-V characteristic showed that the inversion layer could not respond to the ac signal in dark. Also the interface states in minority carrier band gap half could not respond to the ac signal in dark beyond -0.50 V. The low frequency C-V characteristics under illumination show the presence of interface state density peak, as was observed in other samples under illumination. The oxide thickness calculated from oxide capacitance was found to be 537 Å. The bulk doping density in silicon was found to be 5.0×10^{11} cm^{-3} and corresponding bulk Fermi level potential was 0.23 V.

Figure 4.25 displays dark space charge capacitance, C_{scd}, vs interface potential, Ψ_i, characteristic for sample CNOT 47 calculated from experimentally obtained doping density. The

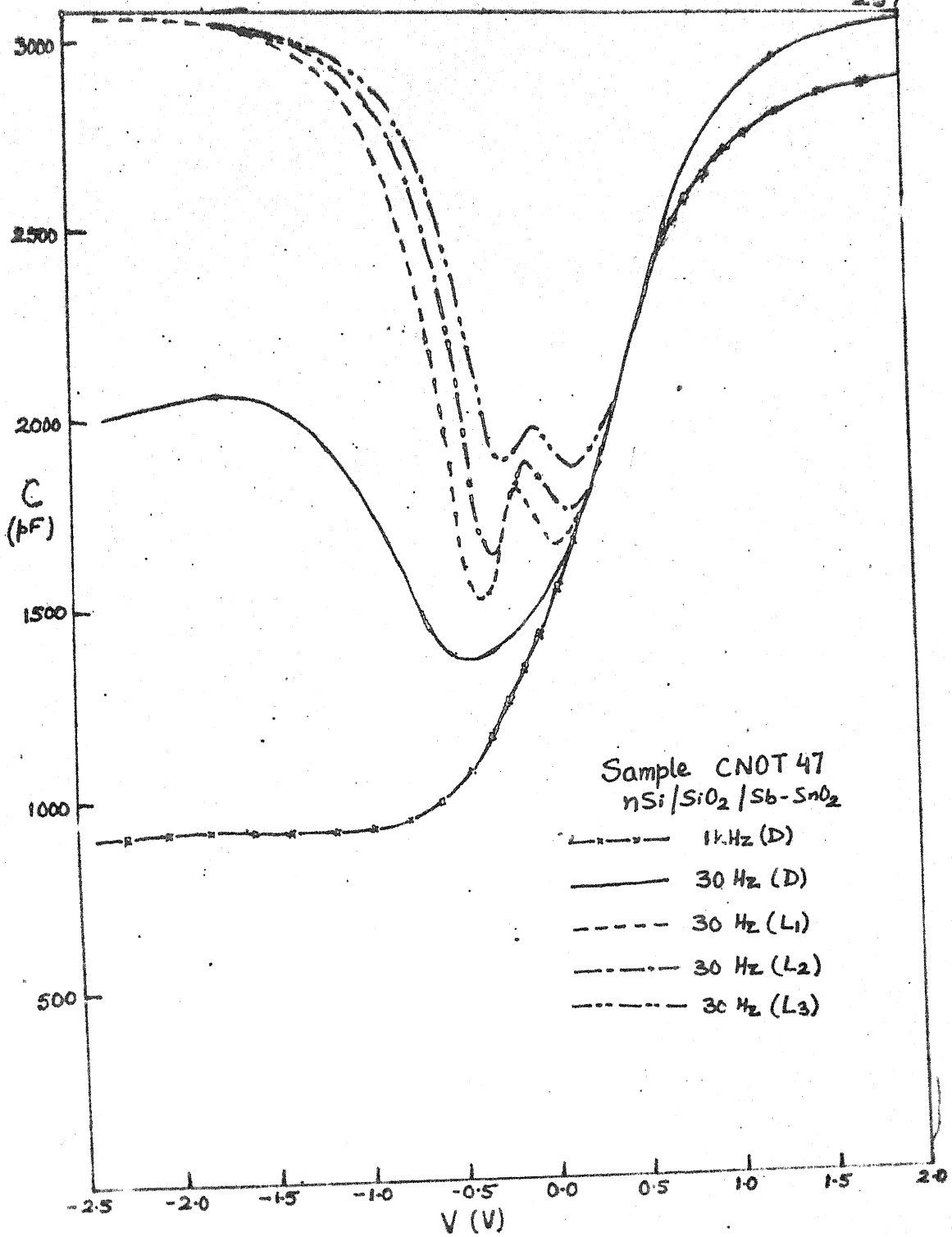


Figure 4·24 A selection of capacitance vs voltage characteristics of a typical chemical vapor deposited Sb doped SnO_2 - SiO_2 - Si device, sample CNOT 47, in dark and under illumination levels L1, L2, and L3

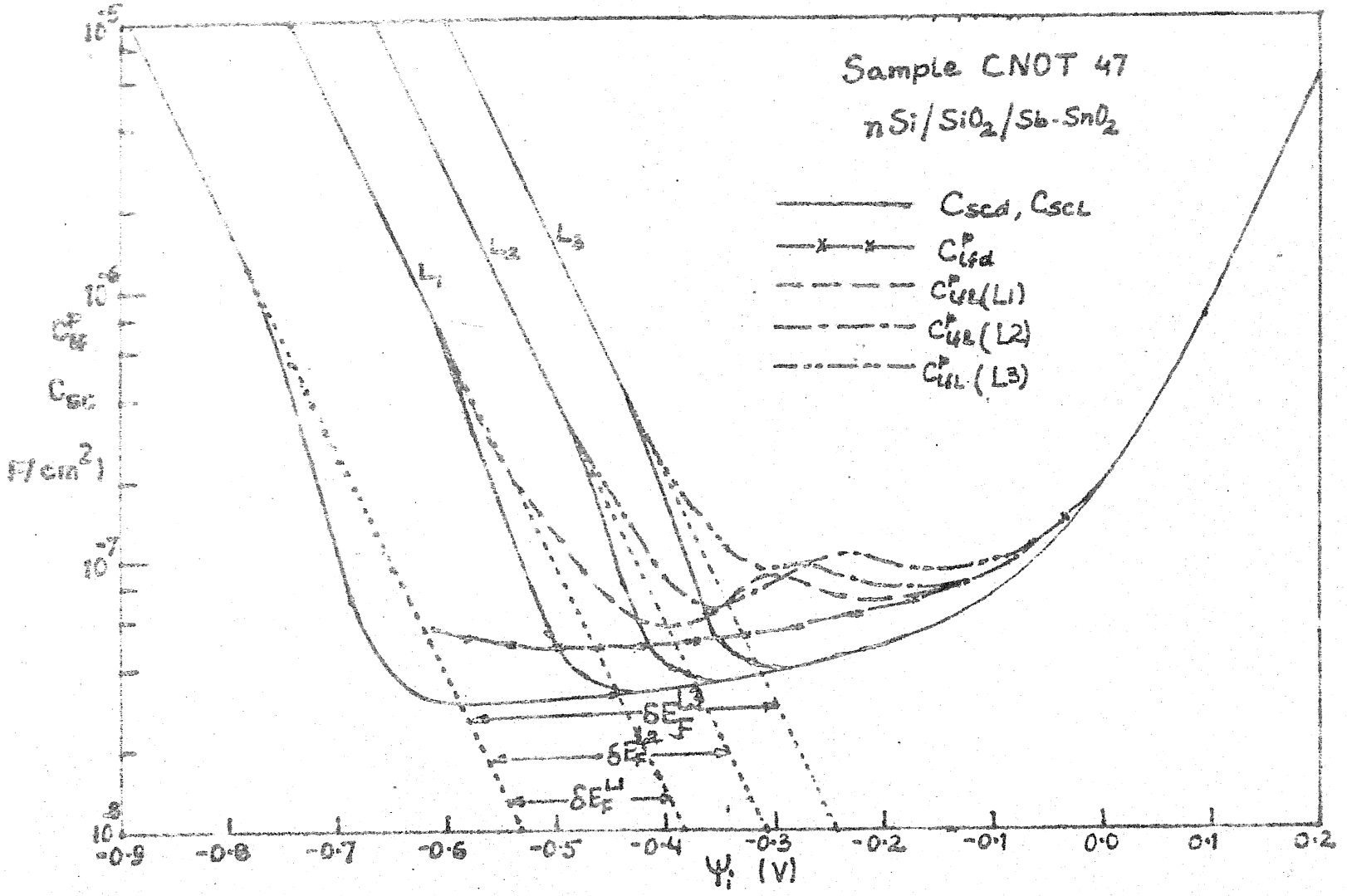


Figure 4.2$\frac{1}{2}$ Semilogarithmic plot of experimental C'_{lf} vs ψ_i and calculated C_{sc} vs ψ_i characteristics of sample CNOT-47 in dark and under illumination levels L_1, L_2, and L_3

experimental low frequency equivalent parallel capacitance vs Ψ_i characteristics for the illumination levels of zero, L_1,L_2, and L_3 are also plotted in Figure 4.25. The parallel capacitance in dark was obtained in accumulation, depletion and weak inversion regions, but could not be obtained in strong inversion as the inversion layer could not respond to 30 Hz ac signal in dark. The quasi-Fermi level separation for illumination levels L_1,L_2, and L_3 were calculated from parallel shift in ln C^p_{lfl} vs Ψ_i plot in strong inversion, and these were found to be 0.15 eV, 0.22 eV and 0.29 eV respectively for illumination levels L_1,L_2,L_3. Consequently, space charge capacitance under light, C_{scl} was calculated using values of quasi-Fermi level separation at each illumination level. C_{scl} vs Ψ_i characteristics at these three illumination levels are also displayed in Figure 4.25. It is seen that the dark parallel capacitance in case of sample CNOT 47 did not show any peak, while illuminated parallel capacitance curves showed peaks close to valence band edge which were identified to be due to charge exchange between valence band and hole imref.

Figure 4.26 displays the interface state density distribution in sample CNOT 47 obtained in dark and under illumination levels L_1,L_2, and L_3. The interface state density distribution in dark showed a very shallow U shaped profile in the energy region of 0.30 - 0.75 eV above valence band, with mid gap state density of about $1x10^{11}$ cm^{-2} V^{-1}. The state density profile in

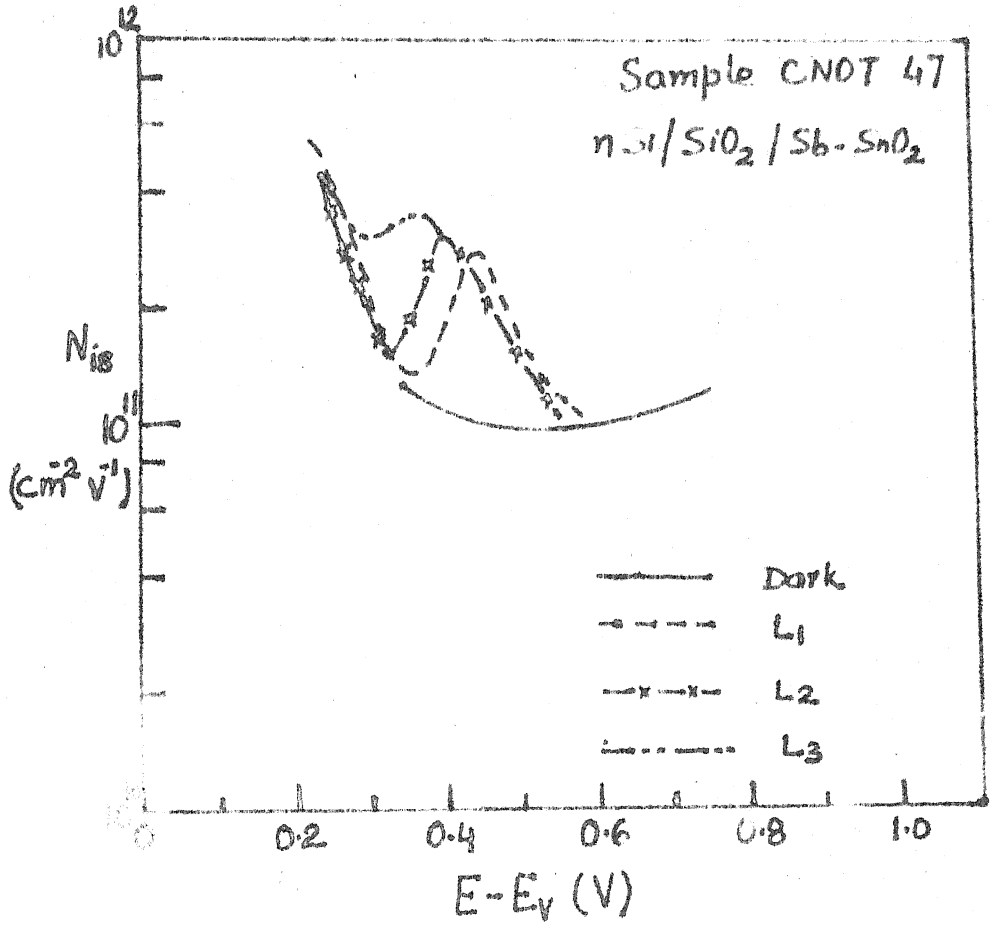


Figure 4.26 Experimental interface state density, N_{is}, as a function of band gap energy, E_1 for sample CNOT-47 obtained from the C-V characteristics in dark and under illumination levels L_1, L_2 and L_3

dark did not show any peak or hump and the values of state density at 0.75 eV above valence band was only 1.2×10^{11} cm^{-2} V^{-1}. Comparing interface state density profiles of samples SNOI 3 (cf. Figures 4.17, SPOI 1 (cf Figure 4.20), CNOT 51 (cf Figure 4.23) and CNOT 47 (Figure 4.26) it is observed that in all cases illumination gives rise to interface state density peak near valence band whose magnitude increases with illumination level and position shifted towards valence band edge. The origin and nature of these states could not be ascertained. These peaks were located in the range of 0.30 - 0.35 eV above E_v for spray deposited In_2O_3 samples and 0.35 - 0.45 eV above E_v for chemical vapor deposited SnO_2 samples.

4.4.3 Electron-Beam Deposited TCOS Structures

Electron-beam deposition of In_2O_3 has been used to fabricate TCOS structures on n-type and p-type silicon. Interface investigations in these samples have been carried out using capacitance and conductance techniques under illumination.

Figure 4.27 displays a selection of capacitance vs voltage characteristics of a typical In_2O_3-SiO_2-nSi device, sample ENOI-16, measured at different frequencies in dark and under illumination levels L_1, L_2, and L_3. It is seen that the states in the minority carrier band gap half and the inversion layer could not respond to the 30 Hz ac signal in dark, but

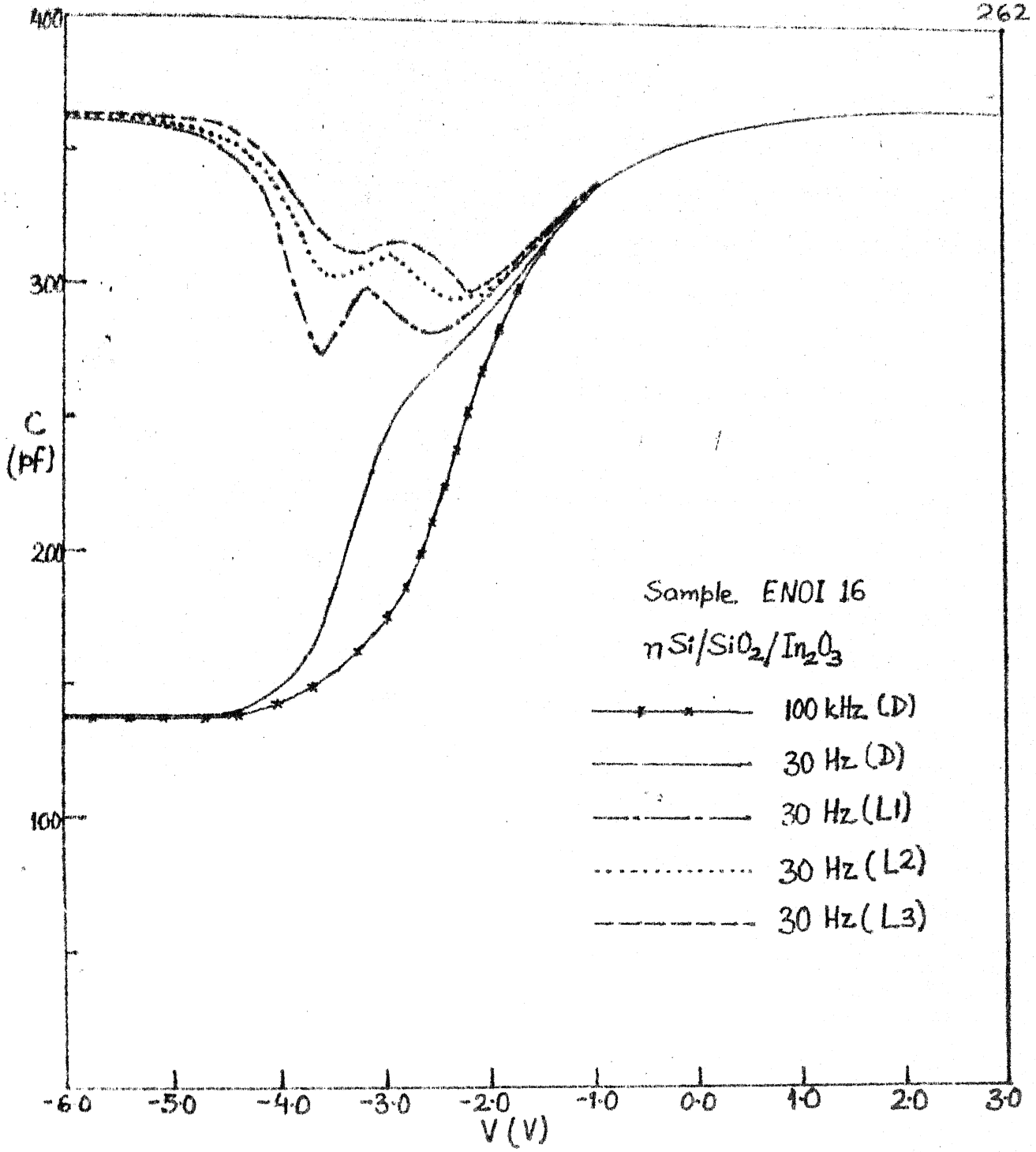


Figure 4.27 A selection of capacitance-voltage (C-V) characteristics of a typical e-beam deposited Sn doped In_2O_3-SiO_2 -nSi device, sample ENOI-16, measured at different frequencies and in dark and under illumination levels L_1, L_2 and L_3

they responded to the same under illumination. The illuminated capacitance approached oxide capacitance value in strong inversion and in strong accumulation. No dispersion was observed between 30 Hz and 120 Hz illuminated C-V characteristics and hence 30 Hz illuminated C-V characteristics were considered as t the low frequency equilibrium characteristics. The oxide thickness was found to be 733 Å. The donor density, N_D, was found to be 5.0×10^{15} cm^{-3} and the corresponding bulk Fermi potential was calculated as 0.23V.

Figure 4.28 displays space charge capacitance in dark, C_{scd} calculated using experimentally obtained doping density for sample ENOI-16. Low frequency (30 Hz) C-V curves at each illumination level were graphically integrated to obtain corresponding ψ_i vs V relationships. Experimentally obtained low frequenc parallel capacitance, C^p_{lf}, for sample ENOI-16, at each illumination level are also presented in Figure 4.28. Low frequency parallel capacitance curves under illumination show a peak near valence band edge. The imref separation was found to be 0.12 eV, 0.23 eV, and 0.30 eV for illumination levels L_1, L_2, and L_3, respectively. Subsequently, space charge capacitance at different illumination levels were calculated and plotted in Figure 4.28.

Figure 4.29 presents interface state density profile of sample ENOI-16 obtained from capacitance data analysis in dark and under illumination. The issue of electron vs hole exchange

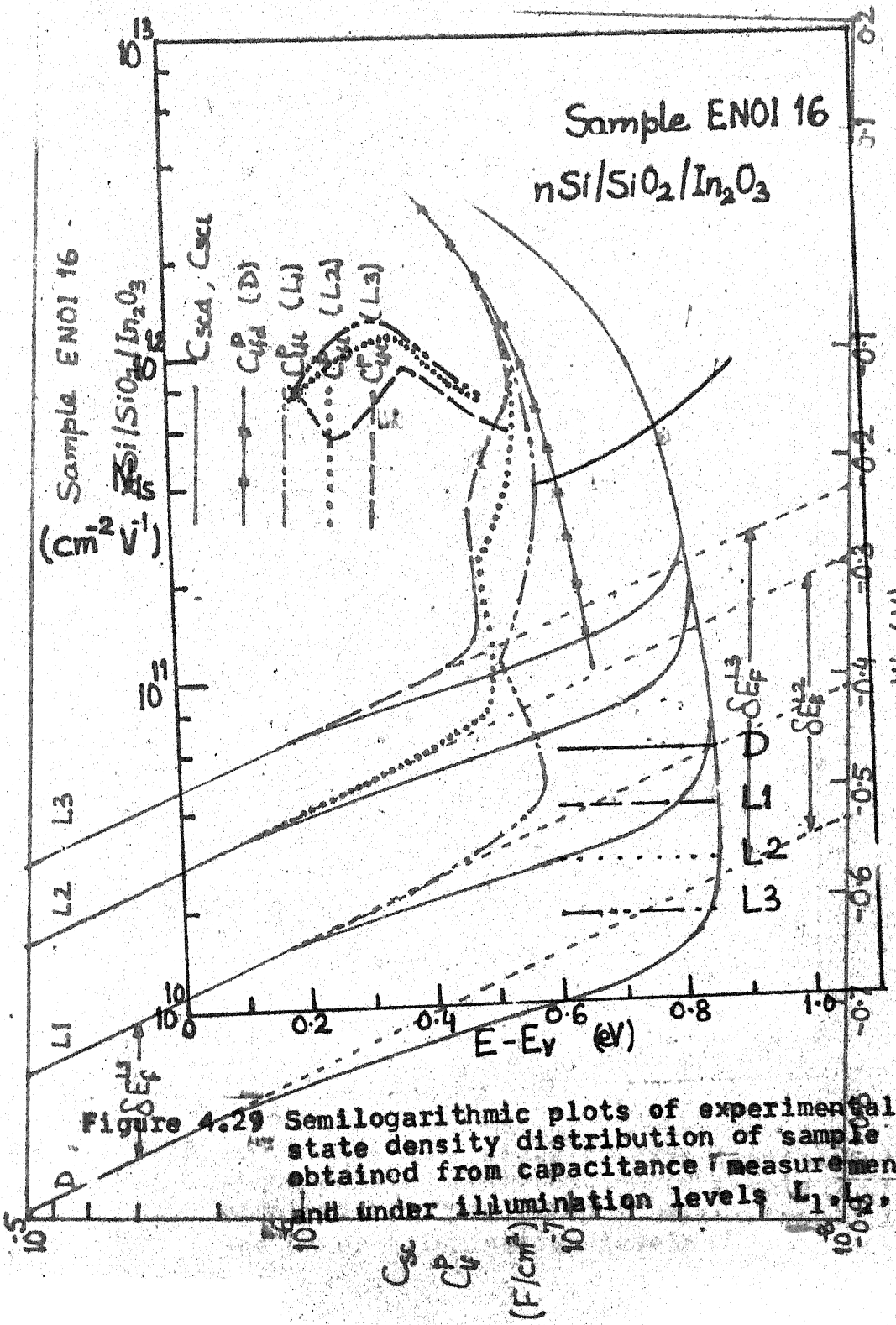


Figure 4.28 Semilogarithmic plot of experimental C_{sc} and calculated C_{sc} vs ψ_s characteristics of sample ENOI-16, in dark and under illumination levels L_1, L_2, and L_3

Figure 4.29 Semilogarithmic plots of experimental interface state density distribution of sample ENOI-16 obtained from capacitance measurements in dark and under illumination levels L_1, L_2, and L_3

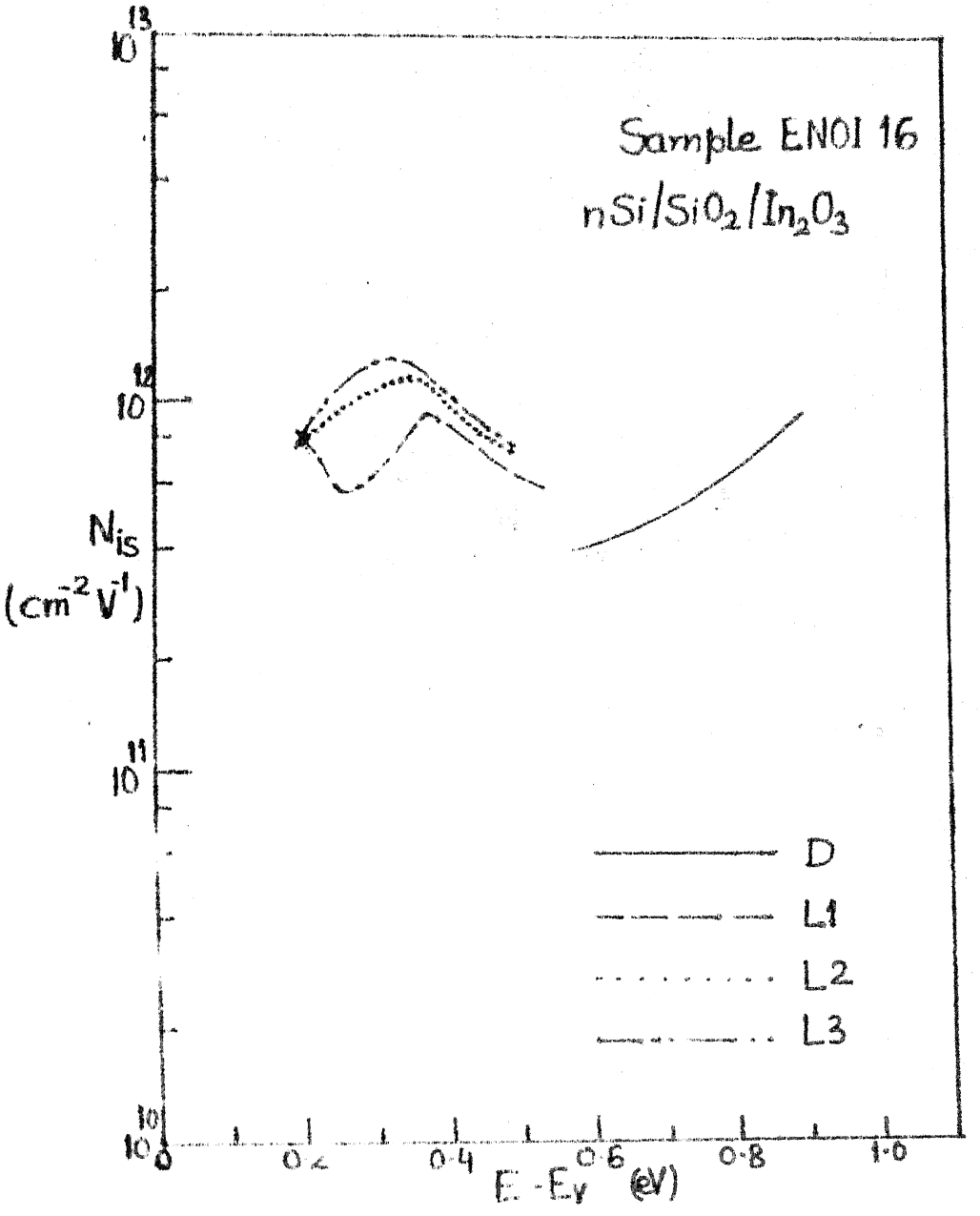


Figure 4.29 Semilogarithmic plots of experimental interface state density distribution of sample ENOI-16 obtained from capacitance measurements in dark and under illumination levels L_1, L_2, and

at the states was resolved as explained in Section 4.3.1 in case of non-availability of experimental capture cross-section data. The state density profile in upper half band gap, obtained in dark and under illumination, indicated a U shaped background with midgap value of density of states as 4.0×10^{11} cm^{-2} V^{-1}. The state density distribution in lower half band gap could not be obtained in dark as these states could not respond to 30 Hz ac signal used. However, under illumination, these states responded to the applied signal and interface state density distribution could be obtained. Illumination level L_1 revealed a peak located at 0.37 eV above valence band. The magnitude of this peak was about 9.3×10^{11} $cm^{-2}V^{-1}$. As observed in case of spray and chemical vapor deposited samples, the magnitude of the peak increased with light intensity and its location shifted towards valence band edge. Under illumination level L_3, the peak was located at 0.33 eV above valence band and its magnitude was 1.3×10^{12} $cm^{-2}V^{-1}$.

Figure 4.3 presents a selection of C-V characteristics of a typical In_2O_3-SiO_2-pSi device, sample EPOI-7, measured at different frequencies, and in dark and under illumination levels L_1, L_2, and L_3. It is seen from Figure 4.3 that 30 Hz illuminated capacitance approached oxide capacitance value in strong accumulation and strong inversion, but 30 Hz dark capacitance showed dispersion in inversion. No dispersion was observed in illuminated capacitance data at 30 Hz and 120 Hz and hence the 30 Hz

illuminated capacitance vs voltage characteristics were considered as low frequency equilibrium characteristics. The oxide thickness calculated from oxide capacitance was 678 Å. The acceptor density, N_A, was found to be 1.25×10^{16} cm^{-3} and the corresponding Fermi potential in bulk was found to be 0.17 V.

Figure 4.4 displays space charge capacitance in dark, C_{scd}, calculated using experimentally obtained doping density for sample EPOI-7. Low frequency (30 Hz) capacitance vs voltage curves at each illumination level were graphically, integrated to obtain ψ_i vs V characteristics which have been presented in Figure 4.5. Low frequency parallel capacitance, C^p_{lf}, at each illumination level were calculated from the measured C-V curves at low frequency, and these have been displayed in Figure 4.4. The quasi-Fermi level separation for sample EPOI-7 under illumination levels L_1, L_2, and L_3, obtained from three different methods suggested in Section 4.3, have been presented in Table 4.1. The imref separation was found to be about 0.25 eV, 0.32 eV, and 0.47 eV for illumination levels L_1, L_2, and L_3 respectively. Subsequently, space charge capacitance at different illumination levels were calculated and plotted in Figure 4.4. The C-V and C^p_{lfl} vs ψ_i characteristics reveal two peaked state density distributions, one near valence band and the other near conduction band.

Interface state density profiles for sample EPOI-7 obtained from capacitance data in dark and under different illumination

levels have been presented in Figure 4.6. Dark capacitance data of sample EPOI-7 showed a broad N_{is} peak located around 0.38 eV above valence band edge. Under illumination, the magnitude of the peak increased, the width of the peaked density distribution became smaller, and its location shifted towards valence band edge with increase in light intensity indicating presence of optically assisted states. The state density at the peak near valence band under illumination level L_3 was 1.1×10^{12} cm^{-2} V^{-1}. Sample EPOI-7 revealed an additional very sharp peak at about 0.30 eV below conduction band edge under illumination level L_1. The magnitude of the peak near conduction band edge also increased with light intensity and its position shifted towards conduction band edge. The magnitude of the peak near conduction band was larger by about one order of magnitude compared to that for the peak near valence band edge. Under illumination level L_3, the magnitude of the peak near conduction band was 1.6×10^{13} cm^{-3} V^{-1}. This peak was not observed in dark. This sample therefore shows the presence of additional optically assisted states near conduction band.

Figures 4.8 and 4.13 show semilogarithmic plots of conductance vs voltage characteristics of sample EPOI-7 at different frequencies, in dark and under illumination level L_1, respectively. Corresponding $G_{p/\omega}$ vs V characteristics in dark and under illumination level L_1 are shown in Figures 4.9 and 4.14 respectively. Experimental $G_{p/\omega}$ vs ω characteristics of sample EPOI-7 at various values of

the bias and illumination levels are shown in Figure 4.10. The $G_{p/\omega}$ vs ω plots indicate that the states belonging to the peaked state density distribution near valence band in dark could be represented by continuum of states under the influence of statistical fluctuation in interface potential. However, under illumination, single level states also contributed to the peaked density distribution near valence (cf. Figure 4.10). Figure 4.10 also reveals that the peaked state density distribution near conduction band under illumination consisted of single level states. The states responding to optical illumination, therefore, appear to be single level states.

The issue of hole vs electron exchange with states was resolved easily for sample EPOI-7 by obtaining capture cross-sections for holes, σ_h, and for electrons, σ_e, at different interface potentials, from the experimentally obtained $\sigma_{p/\omega}$ vs V or $G_{p/\omega}$ vs ω characteristics at different frequencies in dark and under illumination. The occupancy of states was found to be controlled by hole imref in dark, and under illumination for the states under peaked density distribution near valence band, since for this interface potential range $p_s \cdot \sigma_h > n_s \cdot \sigma_e$. Similarly, electron imref was found to control the occupancy of states under peaked density distribution observed under illumination near conduction band.

Interface state densities at different interface potentials obtained by conductance technique in dark and under illumination are also presented in Figure 4.6. Excellent matching between the state densities obtained from conductance and capacitance techniques even at the peaks indicates that the capacitance data under illumination have been properly analysed. This lends confidence in capacitance data analysis technique under illumination presented in Section 4.3.1.

The admittance data analysis of sample EPOI-7 under illumination made it possible to obtain electron capture cross-section, σ_e, of upper half bandgap states, and hole capture cross-section, σ_h, of lower half bandgap states. Figure 4.12 presents experimentally obtained state capture cross-sections for holes, σ_h, and for electrons, σ_e, for sample EPOI-7. Figure 4.12 indicates that hole capture cross-sections were in the range of 10^{-16}-10^{-15} cm^2, while electron capture cross-sections were in the range of 10^{-20} - 10^{-18} cm^2. Moreover, for these optically assisted states, the capture cross-sections were found to vary strongly with band energy and illumination level (cf. Figure 4.12).

Surface admittance data analysis of sample EPOI-7 under illumination demonstrates that with careful measurements, capacitance and conductance techniques under illumination can be used to obtain reliable information about interface states. It also demonstrates that both capacitance and

conductance data analysis are necessary for obtaining reliable results under illumination especially since capture cross-sections may not be equal for holes and electrons, as was found in case of sample EPOI-7. Moreover, the conductance technique was found to give additional information about the states which could be helpful in determining the nature and origin of states.

4.4.4 Effect of Illumination and Processing on State Density Distribution

Irrespective of the deposition method used, the TCOS samples revealed a peaked interface state density distribution under illumination near valence band edge overlying a U shaped background. The peaks were located in the region of 0.30-0.45 eV above valence band, their magnitude increased with light intensity, and their location shifted towards valence band edge.

Interface investigations on thermally grown SiO_2-Si system, without a subsequent anneal, have been reported to give a broad peaked interface state density distribution located around 0.30 eV above valence band [34-36]. We have also employed unannealed thermally grown SiO_2-Si system for TCOS samples and obtained a peak in the same band energy region in all the samples. This peak therefore appears to be due to an inherent interface defect in thermally grown SiO_2-Si interface. Theoretical studies have attributed such a peak to silicon

dangling bands at the interface [37]. Post oxidation annealing in a mixture of H_2 and N_2 around 450°C anneals out these states, and hence finished devices which undergo such a heat treatment after metallization show only a U shaped density distribution.

The reported investigations have been carried out in dark and the effect of illumination on the peaked state density distribution has not been studied. We have also obtained the peaked state density distribution around 0.38 eV above valence band in dark in case of e-beam deposited sample on p-Si, sample EPOI-7. In case of other samples fabricated on n-Si by spray hydrolysis, CVD, and e-beam deposition, the states in lower half of band gap could not respond to the applied 30 Hz ac signal in dark and hence information about these states could not be obtained in dark. Spray deposited sample on p-Si, sample SPOI-1, showed a hump in state density distribution in band energy range of 0.30-0.50eV above valence band, indicating presence of additional states in this region overlying U shaped density distribution.

All the samples showed that the magnitude of state density peak near valence band increased with light intensity and its location shifted towards valence band edge. This indicates towards the existence of optically assisted states in the band energy range of 0.30-0.45 eV above valence band. In optically assisted states, the capture cross-section varied strongly with band energy and illumination level. These states

are not due to permanent photon damage since the behaviour with illumination is reversible. The origin of these states could not be ascertained. However, it appears that they are caused by some optically assisted reversible process. In case of sample EPOI-7, in which case conductance technique could be used for admittance data analysis, it was found that $\sigma_h >> \sigma_e$.

Spray deposited and chemical vapor deposited samples did not reveal any peaked density distribution in upper half of the band gap. Electron-beam deposited sample on p-Si, sample EPOI-7, however, revealed a very sharp peak located in the range of 0.31-0.18 eV below conduction band under illumination. This peak also appears to be due to optically assisted states since the magnitude of the peak increased with illumination level while its location shifted towards conduction band edge. Conductance technique revealed these states to be single level states. These states could have been generated due to radiation damage during e-beam deposition.

In view of the possibility of existance of optically assisted states, interface state investigation under illumination becomes important for all opto-electronic devices which operate under optical illumination.

Physical deposition processes involving energetic particles are found to cause radiation damage which can be annealed with suitable heat treatments [2-13]. Processes involving energetic electrons have been found to create additional

interface states probably due to ionization by energetic electrons and X-rays [2-9]. Irradiation by electron beam has been found to reveal, by capacitance technique, a peak around 0.30 eV below conduction band with magnitude in the range of 10^{12}-10^{13} $cm^{-2}V^{-1}$ [8,10]. With increase in electron dose, the magnitude of this peak has been reported to increase and its position shifted towards conduction band edge [8]. 'DLTS measurements have revealed a peak located around 0.10 eV below conduction band,with magnitude of the order of 10^{12} $cm^{-2}V^{-1}$, for the same sample which showed a peak around 0.30 eV below conduction band by capacitance technique [8]. Electron capture cross-section for these states has been reported around 10^{-19} cm^2 [8], which matches with the values obtained by us. In addition to damage at the interface, the electron beam has been found to generate traps in SiO_2 [6]. The capture cross-sections associated with these electron trapping centres show strong field dependence, probably due to distribution of these traps along normal to the interfacial plane in the oxide [6]. Sample SPOI-7 also revealed a peak in the range of 0.31-0.18 eV below conduction band whose magnitude increased from about 10^{12} to 10^{13} cm^{-2} V^{-1} with light intensity and whose position shifted towards conduction band edge. These states could have been generated by stray electrons reaching interface. Field dependence of electron capture cross-section also indicates the possibility of traps distributed in oxide as has been reported in literature [6].

Except the peak near conduction band edge, the state density distributions obtained in TCOS samples prepared by the three deposition methods are similar in form, although magnitudes differ . Spray deposited samples showed minimum interface state density around 8×10^{10} cm^{-2} V^{-1} at the mid gap, while e-beam deposited samples showed maximum density of states around 4×10^{11} cm^{-2} V^{-1} at the mid gap. Chemical vapor deposited samples showed mid gap state density around 1×10^{11} cm^{-2} V^{-1}.

4.5 CONCLUSIONS

We have demonstrated that interface state investigation using transparent conductor-oxide-semiconductor(TCOS)device under illumination extends the capabilities of admittance techniques and makes it possible to obtain interface state density distribution in most of the band gap. We have developed a procedure for the capacitance and the admittance data analysis under illillumination which gives reliable interface state density distribution. Three direct methods have been presented for determining quasi-Fermi level separation under illumination, which involve either high or low frequency capacitance data in inversion. We have also demonstrated that though in dark the capacitance data can be analysed independently to obtain interface state density distribution, under illumination the capacitance and the conductance techniques are to be used together for obtaining reliable information about interface states. The capacitance data gives quasi-Fermi level separation under

illumination, while the admittance data under illumination gives capture cross-sections for majority carriers and minority carriers. The knowledge about capture cross-sections becomes necessary to determine which imref controls occupancy of states, especially if $\sigma_h \neq \sigma_e$, as was obtained for e-beam deposited sample. The occupancy of states is controlled by the hole imref if $p_s\sigma_h >> n_s\sigma_e$, otherwise electron imref will dominate. In the absence of experimental data on state capture cross-sections, the issue of hole vs electron exchange can be resolved in the following manner. The states near a band edge will exchange charge with the corresponding band. If $\sigma_h = \sigma_e$ and does not vary with band energy, than the occupancy of states will be controlled by the imref which is closer to the respective band edge. If $\sigma_h \neq \sigma_e$, or they vary with band energy, then there will be uncertainity about the dominant imref, for interface potential region of about 0.12 V on each side of the interface potential at which both the imrefs are equidistant from the mid gap energy level. This is on the basis of the assumption that the capture cross-sections normally will not vary by more than four orders of magnitude. In such a case interface state density is not calculated in this potential range. If a peak is obtained in state density distribution, then all the states corresponding to the peaked distribution will exchange charge with the band with which the states at the peak exchange charge. This simplifies the

resolution of the issue of hole vs electron exchange with states. Excellent matching in interface state densities obtained by the capacitance and the conductance techniques under illumination show that the capacitance and the admittance data under illumination are properly analysed. This lends confidence in the analysis procedure developed.

Interface state density distributions in case of TCOS samples prepared by spray hydrolysis, chemical vapor deposition, and e-beam deposition reveal the presence of optically assisted states with a peaked density distribution near valence band overlying a U shaped background. The peak is located in the band energy region of 0.30 - 0.45 eV above valence band. The magnitude of the peak increased with light intensity and its position shifted towards valence band edge. These states could be due to silicon dangling bonds at the interface which are characteristic of thermally grown SiO_2-Si interface.

Amongst the three deposition processes used, e-beam deposited samples showed maximum density of states (around 4×10^{11} $cm^{-1}V^{-1}$) at the mid gap while spray deposited samples showed minimum density of states at the mid gap, around 8×10^{10} $cm^{-2}V^{-1}$. The nature of state density distribution was same in all the cases except that the e-beam deposited sample on p-Si revealed additional optically assisted states with a peak in the range of 0.31-0.18 eV below conduction band edge. The

magnitude of the peak was in the range of 10^{12} cm^{-2} V^{-1} and it increased with light intensity and its position shifted towards conduction band edge. These states could be due to radiation damage due to e-beam deposition. Electron capture cross-sections for the states giving peaked distribution near conduction band was in the range of 10^{-20}-10^{-18} cm^2 which matches with the value of 10^{-19} cm^2 for such states reported in literature. The capture cross-sections have been found to very strongly with band energy and with illumination level in case of optically assisted states.

The origin of optically assisted states could not be ascertained. These are not due to permanent photon damage as the effect of illumination is found to be reversible. These states seem to be generated by some process involving interaction with photons.

References

1. S.M. Sze, 'Physics of Semiconductor Devices', (Wiley, New York 1981).

2. S.T. Pantelides, ed., 'The Physics of SiO_2 and its Interface (Pergamon, New York 1978).

3. R.A. Gdula, IEEE Trans. Electron Devices ED-26, 644 (1979).

4. D.V. Mccaughan, and R.A. Kushner, Proc. IEEE 62, 1236 (1974).

5. D.R. Collins, and C.T. Sah, Appl. Phys, Letters 8, 124 (1966).

6. T.H. Ning, J. Appl. Phys. 49, 4077 (1978).

7. H.S. Lee, IEEE Trans. Electron Devices ED-25, 795 (1978).

8. M. Pockerar, R. Fulton, P. Blaise, D. Brown, and R. Whitlock, J. Vac. Sci. Technol 16, 1658 (1979).

9. G. Lucovsky, S.T. Pantelides, and F.L. Galeener, eds., 'The Physics of MOS Insulators' (Academic, New York, 1980).

10. G.A. Scoggan and T.P. Ma, J. Appl. Phys. 48, 294 (1977).

11. S.W. Pang, D.P. Rathman, D.J. Silversmith, R.W. Mountain, and P.D. DeGraff, J. Appl. Phys, 54, 3272 (1983).

12. A.K. Sinha, J. Electrochem. Soc. 123, 65 (1976).

13. S. Alexandrova, K. Kirov, and A. Szekeres, Thin Solid Films 75, 37 (1981).

14. E.H. Nicollian and J.R. Brews, 'MOS Physics and Technology', (Wiley, New York, 1982).

15. L.N. Terman, Solid State Electron. 5, 285 (1962).

16. C.N. Berglund, IEEE Trans. on Electron Devices ED-13, 701 (1966).

17. M. Kuhn, Solid State Electron 13, 873 (1970).

18. P.V. Gray and D.M. Brown, Appl. Phys. Letters 8, 31 (1966).

19. E.H. Nicollian and A. Goetzberger, Bell Syst. Tech. J. 46, 1055 (1967).

20. P. Su, A. Sher, Y.H. Tsuo, J.A. Moriarty and W.E. Miller, Appl. Phys. Lett. 36, 991 (1980).

21. A. Sher, Y.H. Tsuo, P. Su, W.E. Miller, in ref. 9 p.236.

22. T.C. Poon and H.C. Card, J. Appl. Phys. 51,5880 (1980).

23. T.C. Poon and H.C. Card, J. Appl. Phys. 51,6273 (1980).

24. S. Kar, S. Varma, P. Saraswat, and S. Ashok, J.Appl. Phys. 53, 7039 (1982).

25. S. Kar, and S. Varma, J.Appl. Phys. 54, 1988 (1983).

26. S. Kar, and S. Varma, To be published.

27. D.K. Schroder, IEEE Trans. Electron Devices ED-25, 90 (1978).

28. L.L. Thompson, D.H. McCann, R.A. Tracy, F.J. Kub and M.H. White, IEEE Trans. Electron Devices ED-25, 132(1978).

29. D.H. McCann, A.P. Tulrley, J.A. Hall, J.M. Walker, R.A. Tracy and M.H. White, Proc. Int. Solid State Circuits Conf., 30 (1978).

30. D. Brown, M. Ghezzo and M. Garfinkel, IEEE J. Solid State Circuits SC-11, 128 (1976).

31. D. Brown, M. Ghezzo and P.M. Sargent, IEEE Trans. Electron Devices 25, 79 (1978).

32. T. Ando, and C.K. Fong, IEEE Trans. Electron Devices ED-29, 1161 (1982).

33. S. Ashok, P.P. Sharma, and S.J. Fonash, IEEE Trans. Electron Devices ED-27, 725 (1980).

34. N.M. Johnson, D.K. Biegelsen, and M.D. Mayer, in ref.9, p. 311.

35. N.M. Johnson, D.J. Bartelink, and M. Schulz, in ref.2,p.421.

36. N.M. Johnson, D.J. Bartelink, and J.P. McVittie, J. Vac. Sci. and Technol. 16, 1407 (1979).

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